WESTINGHOUSE ELECTRIC CORPORATION
89 Holiday Office Center
Huntsville, Alabama

Final Report

INTEGRATED POWER AMPLIFIER

Contract No. NAS8-11599

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George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Huntsville, Alabama

FOREWORD

This report describes the work accomplished under contract No. NAS8-11599, initiated by the George C. Marshall Space Flight Center, NASA. The work was performed at the Westinghouse Semiconductor Division, Youngwood, Pa.

The project was under the direction of T. C. New, S. Chinowsky, and P. M. Kisinko. Contributors include R. A. Forrest, J. T. Krawczykiewicz and M. F. Amsterdam.

ABSTRACT

Presented is the design and development of an integrated power amplifier, a pair of transistors with associated diodes and resistors encapsulated in an insulated flat package for push-pull amplification operation. The device is intended for space application in power supply systems. Reliability, size and weight, as well as electrical performance, had to be considered. All objectives were achieved.

The report is divided into three principal sections.

1. A summary of the objectives and results, including a survey of the development and recommendations for further work.
2. A detailed presentation of the design and development of the basic device.
3. A discussion of the encapsulation package.

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I. GENERAL SURVEY

A. Objectives

The work was to accomplish the design, development, fabrication and delivery of integrated power amplifiers with the following criteria as objectives:

1. General Requirements:

The physical size is to be as small as possible to meet electrical and mechanical requirements. The amplifier shall not contain more than two slices of semiconductor material. The finished amplifier shall be in one package.

2. Mechanical Specifications:

   a. Hermetically sealed
   b. Semiconductor material to be silicon
   c. Device shall be electrically isolated from case

3. Electrical Specifications:

   a. Suggested circuit configuration given in Figure 1
   b. Push-pull power amplifier
   c. D.C. supply: 28 volts
   d. Input signal: current drive of 1 amp (either side to ground)
   e. Output for input drive: 10 amps
   f. With output driven to saturation at 10 amps, the drop across the driven transistor shall not exceed 1 volt
   g. Time delay plus rise of output for a step input and current gain of 10: less than 6 microseconds
   h. Storage and fall time without back bias and current gain of 10: less than 10 microseconds
   i. Worst-case design to insure meeting above specifications over temperature range -55°C to 150°C
   j. There shall be five leads protruding from the package
      (1) one for each of the two inputs
      (2) one for the power supply negative
      (3) one for each of the two collector outputs

4. Environmental Specifications:

   a. Temperature cycling: -55°C to 125°C, 5 cycles

   b. Moisture resistance: 10 cycles

   c. Centrifugal: 500g

   d. Shock: 500g

   e. Vibration: 250g, 100cps to 2000cps

5. Assumptions:

Based on the above objectives the following factors were proposed:

Item 2a: "Hermetically sealed" was to mean that the encapsulation would have a leak rate no greater than 1×10^{-5} std. cc/min. as determined by a mass spectrograph helium leak test.

Item 3c: With the methods proposed, it was considered that reliability would be insured if the component transistors were capable of operation at a collector-to-emitter voltage of 80 volts min.

Item 3f: The saturation voltage of 1 volt at 10 amps was to be obtained with an input of at least 1 amp.

The voltage requirements were later revised by MSFC to 125V min. In addition, a diode was added to shunt out the E-C circuit. The final design is shown in Figure 2.

The final results have met or exceeded the objectives.

B. Results

The completed integrated power amplifier has the circuit exactly as specified in Figure 2. The package design is shown in Figure 3 and a photograph of the device, in Figure 4.

The final samples delivered have the electrical test results listed in Table I.

Since all test data illustrate terminal characteristics, the gain at lower current, with shunt resistors R_a and R_b appears low, as should be expected. For the same reason, the V_{CEO} and V_{CBO} cannot be measured and are therefore not included in the table.

Although the current rating is given as 10A, the device is capable of current several times higher, as was confirmed by tests conducted by MSFC.

The device was thoroughly tested under all the environmental conditions specified (the results are given in II, G). Since the number of devices fabricated under this limited contract was small, statistically significant data on reliability or meantime between failure figures are not available.

C. Program Development

The basic transistors and fabrication processes had already been developed. Therefore the initial step was to determine the shunt resistance value in order to meet the switching time requirements.

As development progressed, discussions with the contracting agency involving application needs resulted in several modifications. Collector voltage was raised to 125 volts. A damping diode of 1/2 to 3/4 ampere capacity was added. Most important, a more expensive and difficult to construct beryllium-oxide, flat package was found to be desirable (the encapsulation was originally made in a double-ended package, using a glass compression seal). All these modifications were incorporated in the final design.

The contract schedule had to be adjusted to allow for these modifications, especially to permit the development of the beryllia seal, which became a major project. Fortunately, the seal supplier was very cooperative and the difficulties were overcome.

D. Summary and Recommendations

This program has led to the achievement of several milestones in solid state device engineering, including:

1. It pioneers the concept of integrating power semiconductor devices with circuit components.
2. The device design and fabrication demonstrated for the first time that simultaneously diffused technology is compatible with integrated circuits. This is especially valuable for high power application.

3. For the first time in industry, a beryllium oxide insulated flat-package was developed for high power devices.

This device should serve as a basic unit for volume production in view of the large number of applications using push-pull power transistors for either switching or amplifying. The design provides flexibility for scaling either upward or downward depending on the power dissipation of a specific application. The case may similarly be modified to fit particular needs.

It is therefore recommended that further support be considered to accelerate pilot production capability. In addition, the basic concept of power integrated circuits should be applied in other areas where such a need exists.

ORIGINAL CIRCUIT CONFIGURATION

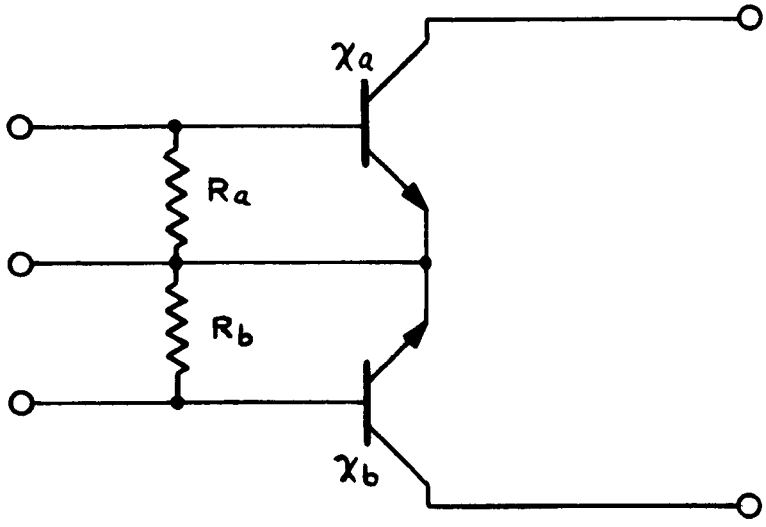


FIGURE - 1

FINAL ELECTRICAL DESIGN

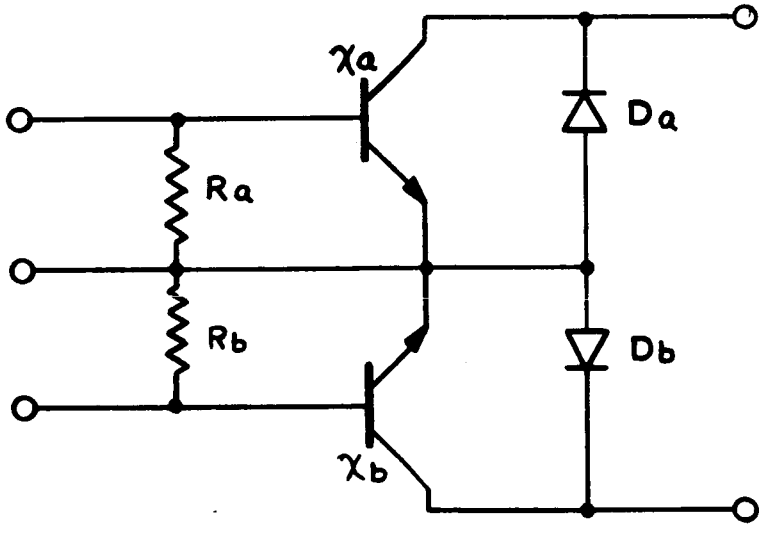
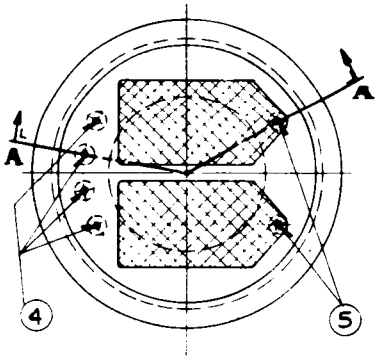
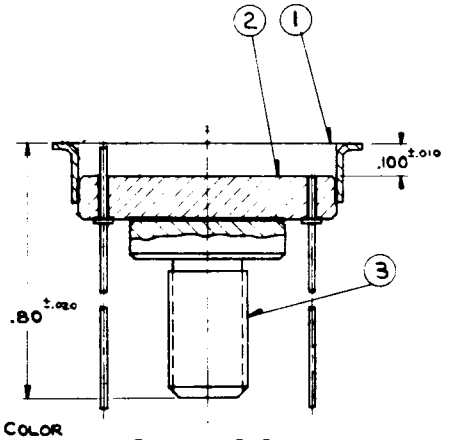


FIGURE - 2

ASM. NOTES:

1. BRAZING MATERIAL MUST HAVE SOFTENING POINT GREATER THAN 580°C.
2. BRAZING MATERIAL NOT PERMITTED ON FLANGE OF EYELET.
3. FINISHED ASM. MUST HAVE A HELIUM LEAK RATE LESS THAN 10^{-8} CC/SEC WITH A DIFFERENTIAL PRESSURE OF 14.5 PSI.
4. BRAZED FILLETS JOINING METAL & CERAMIC PARTS MUST BE CONTINUOUS.
5. MINIMUM CREEPAGE PATH ON CERAMIC BODY BETWEEN METAL PARTS, METALIZED AREAS, OR METAL & METALIZED AREAS AS INDICATED ON DRAWING. (.040 MIN. REF.)
6. CU-CORE LEAD MUST WITHSTAND A MIN. OF FIVE 90° BENDS AT ANY POINT OF LENGTH WITHOUT SURFACE CRACKING OR FATIGUE FAILURE.
7. FLANGE OF EYELET & BASE STUD MUST BE PERPENDICULAR TO EACH OTHER WITHIN .25° T.I.R.

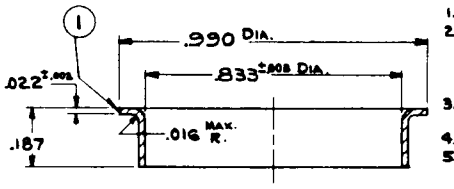




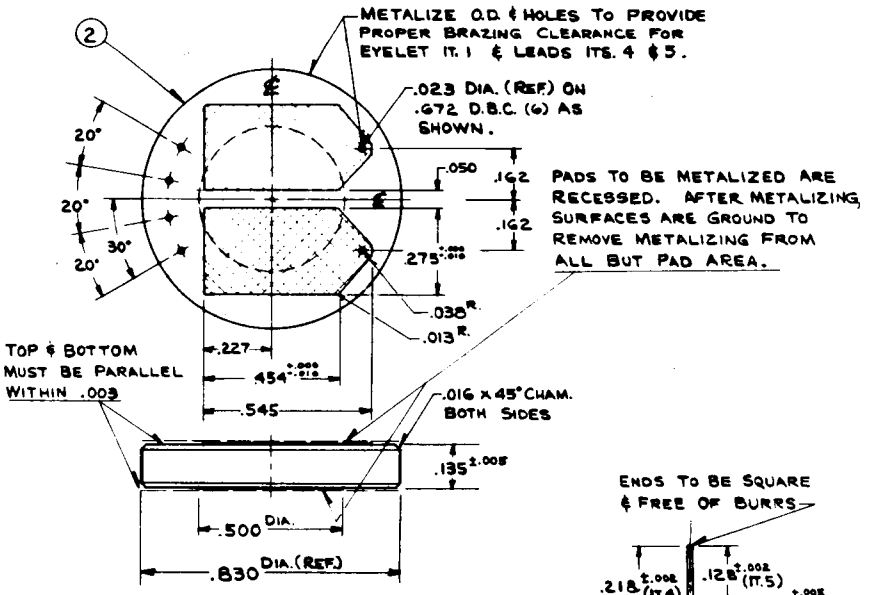
SECTION A-A

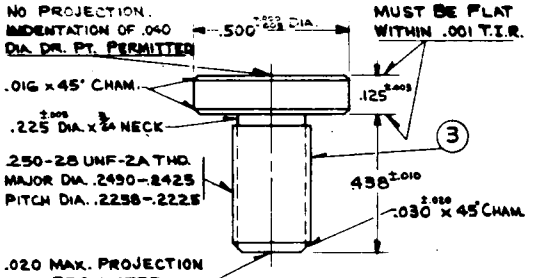
A- OPTIONAL - SEE LEAD DETAIL.
B- CERAMIC MUST HAVE A NATURAL COLOR & BE FREE OF DISCOLORED MARKS.
C- APPLY FINISH 21AA04 (10004±.00015 CU. PL.) ON EYELET AFTER ASSEMBLY.

A	6	WASHER FR. .060 +.004 -.000 x .020 +.004 -.000 x .010 TK. KOVAR	6
	5	LEAD-FR. CU. CORE KOVAR (.007 D. CU & .020 D. Kovar)	2
	4	LEAD-FR. CU. CORE KOVAR (.007 D. CU & .020 D. Kovar)	4
	3	BASE-FR. 1/2 DIA. CU. 1340 GCT (TE. CU.)	1
B	2	INSULATOR- 99.5% OR GREATER BERYLLIA	1
C	1	EYELET-FR. .022 +.003 -.000 TK. STL. SH. 1010 RX	1
Part No.	Item No.	DESCRIPTION & MATERIAL	Req'd

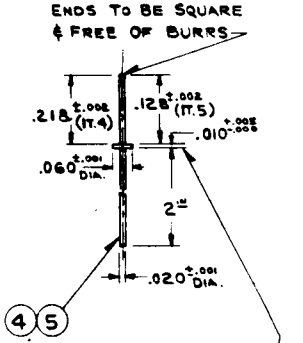


1. MAX. BURR .002
2. NO WRINKLES ALLOWED IN FLANGE. IF SMALL RIBBLES ARE PRESENT IN FLANGE THE CREST TO TROUGH HEIGHT MUST NOT EXCEED .0005 T.I.R.
3. MAX. ALLOWABLE VARIATION OF FLANGE THICKNESS ON ANY INDIVIDUAL PART IS .001.
4. FACES OF FLANGE MUST BE FLAT WITHIN .002 TIR
5. FLANGE MUST BE CONCENTRIC WITH I.D. OF EYELET BODY WITHIN .006 T.I.R.





NOTE: REMOVE ALL BURRS & SHARP EDGES. ▽ ON ALL SURFACES UNLESS OTHERWISE SPECIFIED.



SCALE 4/1=1	DATE	TITLE	CERAMIC-METAL BASE ASSEMBLY, TYPE 179
DRWN. C. Dunn			
CHKD.			
APPD.			
APPD.			
APPD.			
WESTINGHOUSE ELECTRIC CORPORATION SEMICONDUCTOR DEPT. YOUNGWOOD, PA.		C	E.D. Sk. 310276

FIGURE 3

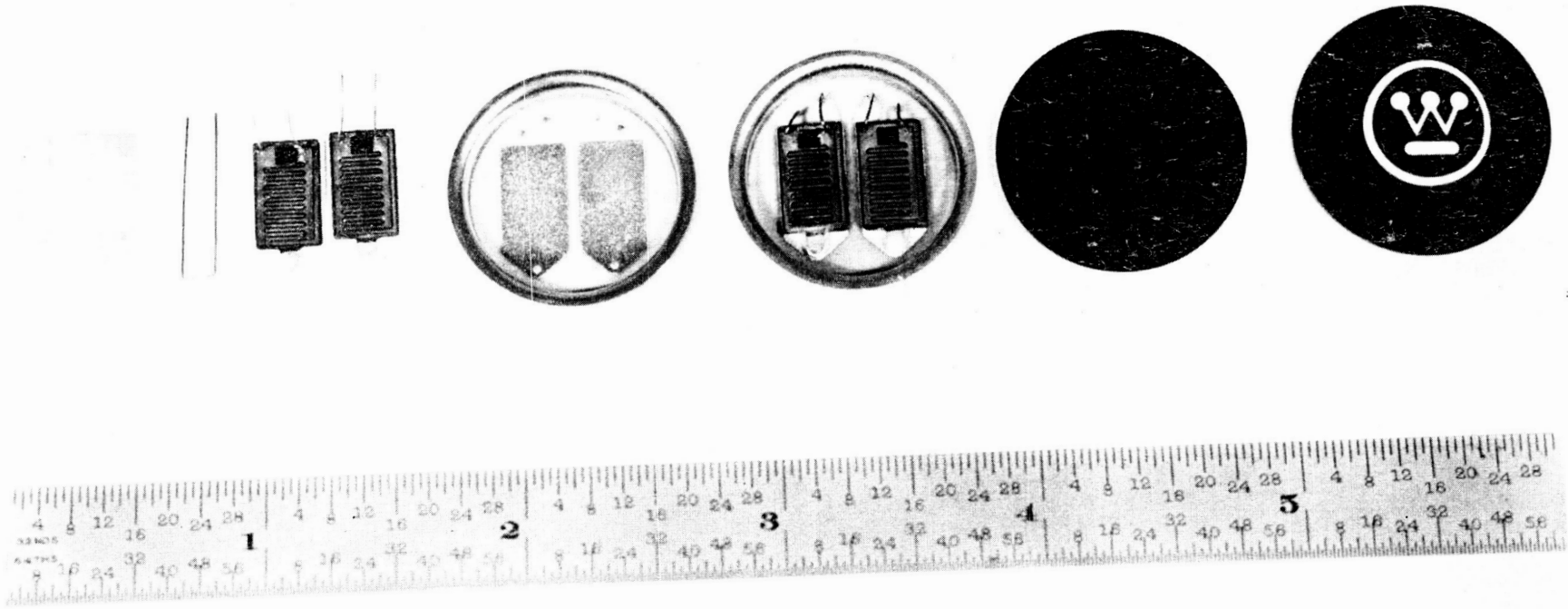


FIGURE 4

Final Device (with components)

TABLE I

SPLIT AMPLIFIER

Final Electrical Test Results

Unit No.	h_{fe} 10A	h_{fe} 5A	V_{CE} (sus)	$V_{CE(sat)}$ 10A	$V_{CE(sat)}$ 5A	$V_{BE(sat)}$ 10A	$V_{BE(sat)}$ 5A	t_{on}/μsec. 10A	t_{on}/μsec. 5A	V_S	t_{off}/μsec. 10A	t_{off}/μsec. 5A
13-1	28.6	27.7	130	1.92	.85	2.50	1.45	3.6	2.1	28.0	11.0	9.6
-2	19.2	20.4	135	1.15	.60	1.75	1.18	2.9	2.5	27.5	9.0	8.8
14-1	33.3	33.3	125	1.53	.50	1.70	1.15	2.2	2.3	27.7	12.0	7.6
-2	29.5	27.0	130	1.15	.60	1.80	1.25	2.2	2.4	28.0	9.5	8.4
16-1	27.0	27.0	135	.98	.55	1.70	1.20	2.6	2.1	28.0	12.5	11.0
-2	25.0	27.8	140	1.03	.55	1.65	1.10	2.9	2.2	27.0	11.5	11.0
18-1	14.9	19.2	125	1.03	.50	1.70	1.15	2.9	2.0	27.5	6.2	6.2
-2	13.0	15.2	130	1.23	.60	1.95	1.13	3.9	4.5	27.5	7.0	5.8
19-1	21.8	25.7	125	1.10	.55	1.80	1.20	2.3	2.5	27.5	9.5	8.6
-2	17.2	26.3	125	1.08	.50	1.75	1.10	2.0	2.3	27.5	8.2	8.0
20-1	16.4	19.6	135	1.20	.50	1.85	1.15	3.2	3.1	27.5	8.2	8.0
-2	27.8	33.3	145	1.23	.57	1.95	1.25	2.2	2.3	27.5	11.0	11.5
21-1	16.1	20.4	130	.95	.50	2.10	1.50	3.5	3.4	27.0	10.5	10.5
-2	20.0	23.3	125	1.15	.60	1.85	1.25	2.5	2.6	27.5	8.5	8.8
22-1	20.0	25.6	130	1.25	.60	2.2	1.40	3.0	2.9	27.5	11.5	12.5
-2	17.6	19.6	140	1.10	.55	1.9	1.25	3.0	2.9	28.0	8.6	8.6
23-1	16.1	20.0	150	1.15	.63	2.25	1.60	3.5	3.3	27.5	9.3	9.2
-2	18.2	21.2	150	.90	.48	1.60	1.20	3.4	2.6	27.5	10.5	10.0
9-1	29.0	30.3	140	1.33	.60	1.93	1.18	3.5	2.1	27.5	12.3	10.0
-2	26.0	25.0	150	1.08	.58	1.70	1.28	3.6	2.0	28.5	11.0	9.4
12-1	48.8	50.0	130	0.80	.43	1.43	1.05	3.4	1.8	27.0	18.5	17.5
	26.3	30.3	130	1.93	.90	2.40	1.54	4.1	1.7	28.0	11.5	10.4

II. DESIGN

A. Introduction

The approach considered most suitable for design of the subject amplifier was to meet the specifications for gain, voltage, and switching speed with adequate safety factors, yet not to exceed these specifications by excessive margins. Reliability is the principal objective dictating this approach. It is well known that secondary breakdown is the major limitation on reliability of power transistors, and it is also generally recognized that secondary breakdown and/or thermal runaway can be minimized by utilizing a device with the lowest possible, but adequate, frequency characteristics. That is, an audio frequency device is more reliable in an audio circuit than a vhf transistor in the same application. Thus, design for the required speed within fairly close limits is more desirable than overdesign for excessive speed. It can also be said, in general, that a device which is designed safely, but not overdesigned, must be more nearly perfect in order to be in specification than one greatly overdesigned. For instance, a transistor designed for 250 volts may contain severe junction or surface defects which could cause instability and failure, yet such a device could still pass a specification for 125 volts. But for a transistor designed for 150 volts to pass tests at 125 volts, imperfections must be insignificant. Similar arguments can be advanced for other device characteristics.

In the interest of minimizing the secondary breakdown and/or thermal runaway, the single or simultaneously diffused transistor SDT structure was selected. In this design, the transistor base region is essentially the virgin silicon crystal. The perfection of the grown ingot is generally considered superior to either diffused or epitaxial material. This is especially true for large areas, where local defects leading to hot spot failure are to be avoided. The SDT structure is also amenable to punch through voltage limited collector design, known to offer superior secondary breakdown protection.

B. Voltage Design

The voltage design was based on the same SDT structure used in Westinghouse transistors WX130 and WX156. These were designed to have the minimum base width to achieve the required frequency and punchthrough between 150 and 200 volts. Calculations were made using Poison's equation with a diffused doping profile. The interaction of doping impurities penetrating from both sides required a correction in evaluating the equations. These corrections were obtained with the aid of a computer. The final results are summarized in Figure 5.

C. Current Gain and Saturation Voltage

In accordance with the "safe" design principle, the component transistors were designed for h_{FE} at 10 amperes to be equal to 20 at 25°C, and not to exceed 15 at 150°C. Current gain greatly in excess of the required value would raise several problems, of which instability due to sensitivity to spurious signals and high collector-emitter leakage current (since $I_{CEO} = h_{FE} I_{CBO}$) are outstanding. With base width and resistivity determined by voltage and speed requirements, design for gain is concerned only with the emitter efficiency. In practice, the limiting factor at high-level operation is the emitter edge length, which can be calculated with good accuracy. In addition to this calculation, the necessary emitter geometry was deduced from experimental results accumulated from Westinghouse's WX130 and WX156 diffused transistors. The emitter geometry is basically the interdigitated type. Saturation voltage, when measured under standard conditions of overdrive of the input, is naturally low for devices with a symmetrical doping profile.

D. Balance

Because of the common-emitter configuration and the large collector current output, it was considered most feasible to fabricate the amplifier by encapsulating two discrete component transistors in the same package, rather than attempt to combine both transistors on a single slice of silicon. Matching of the characteristics of the two transistors was accomplished before final mounting into the encapsulation base.

E. Device Design

The principles discussed in the preceding paragraphs are incorporated here into the physical device. Since the fabrication methods of the simple transistor are well developed, they require no explanation here. Thus, emphasis is placed on the topological modifications that were needed to meet specific structural requirements.

The complete device is built on a piece of silicon .250" x .450". The power transistor is interdigitated and occupies 80% of the area. The remaining 20% of the area is devoted to the resistor and diode. Figure 6 shows the final design.

The base electrode completely circles the emitter, resistor and diode regions so as to avoid surface channel formation. The base fingers are slightly tapered to reduce the injection near the root of the emitter fingers. This minimizes the tendency to generate hot spots.

The diode is beneath the metalized square area at the resistor end. An additional feature is that the diode provides a generous pad for lead attachment. The base end of the resistor is similarly employed as a lead pad, while trimming the shunt resistor to the desired value.

This basic design, although apparently simple, is actually quite sophisticated, permitting some latitude for modifications to meet specific circuit needs. For example, the interdigitals can be amputated or extended for variation in current capacity. The resistance width and length can be changed to satisfy specific circuit applications. Adjustments in diode capacity can similarly be made.

F. Design Development

In this section a number of problem areas involved in design development are discussed. This is followed by a description of the actual fabrication process.

1. Shunt Resistance:

In the initial design the shunt resistor, R_{sh}, and the transistor are both mounted on the same silicon chip but are externally connected. A number of pads were provided to allow for resistance adjustment. (The emitter-base resistor was fabricated with built-in taps allowing optimization of the resistor value depending on the transistor gain.) Isolation of the resistor from the transistor is aided by oxide-masking. Connection of the resistor to the transistor emitter and base contacts was done with jumper wires on the prototype units, but later it was accomplished within the junction or metalizing pattern. The basic device geometry of this initial unit is shown in Figure 7. Figure 8 shows the basic device soldered to the gold-plated molybdenum platform with internal gold-plated silver leads attached.

Table II shows various electrical parameters of several simultaneously diffused transistors. The transistors were tested for switching times using the circuit shown in Figure 9 with various emitter-base shunt resistors. Figures 10 and 11 show turn-on and turn-off times, respectively, as a function of the emitter-base resistor values. From the graphs, it can be seen that the required speed can be achieved with a value of R shunt about 5 ohms, provided h_{FE} is within the approximate range of 10 to 25.

In the final design the resistor was integrated into the transistor unit itself. It was apparent that the choice of resistor taps had already been fixed when the units were ready to be tested. Because of this, and the realization that the resistor value could be varied (upward) by etching, a new mask set was designed (Figure 12 - note tapering of base fingers for minimizing hot spot formation) which provided one minimal resistor value, and also provided integral connections to base and emitter. Prior to this three silver leads had been soldered to the mounted chip -- one to the base contact, one to the emitter, and one connecting two resistor contact pads and the base. After this operation, the free end of the last wire was soldered to the emitter lead and the segment of the wire between resistor contacts was cut (See Figure 13).

2. Diode:

Design was made to have a diode on the same chip with the resistor and transistor. Prior to the incorporation of a diode on the chip, the integrated emitter-base resistor was isolated from the base by a P-N junction. With the diode present the contact metalization connects the emitter and base layers at the diode and a shunting emitter-base resistive path through the base layer between the diode and base metalization appears. Therefore, the oxide masking of the resistor from the "boron atmosphere" during diffusion, which was superfluous in the absence of the diode, was now necessary to avoid very low emitter-base resistance values before etching.

3. Switching:

Table III shows the results of switching tests on an amplifier. The chip was soldered to a molybdenum substrate but had no other provision for heat dissipation. In order to obtain data at reasonable current values, a low duty cycle was employed to keep the necessary heat dissipation rate down. At 5 amperes a total "turn-on" time of 2μsec. was observed while the total "turn-off" time was 8μsec. The storage time, t_s, increases with the base drive, as expected. However, with a maximum base drive of 1 ampere, as specified, the total turn-off time, t_{off}, is 8μsec. which is considerably below the 20μsec, specified at the rated 10 ampere collector current.

4. Fabrication Process:

Below are described the steps taken in fabricating the transistor-resistor chips. These steps can perhaps be better understood if reference is continually made to the process flow chart (Figure 14).

P-type silicon slices of closely matched resistivity are first predeposited with phosphorous (N-type) to a surface concentration greater than 10^{21} using an open-tube, solid source process. The slices are then masked with Kodak Metal-Etch Resist (KMER) and etched with a 15:5:3 etch to form the emitter and resistor geometries. After cleaning, the slices are oxidized

in a steam atmosphere. The resistors of the devices are then masked against the oxide etch and the silicon dioxide removed from the transistor area. After cleaning again, the slices are diffused in a boron atmosphere to drive the emitter and collector, as well as the resistor, to the necessary depth. The boron concentration is such that it does not convert the phosphorous diffused area nor the oxide masked resistor, but forms a low-resistivity base contact region. After lightly sandblasting both sides of the slice, photoresist is again applied to define the contact regions. The slices are then subjected to an electroless nickel plating operation. The masking material is removed, the nickel sintered to improve the adhesion to the silicon, the device remasked, and the same area is nickel plated for a second time. The second KMER mask is removed and the slices are diced into individual units. After a thorough cleaning operation, the device is dipped into a molten bath of solder for a few seconds. The solder adheres only to the nickel plated areas.

Following the above steps, the device is mounted to a gold plated molybdenum platform and silver leads are attached simultaneously. The gold plating protects the molybdenum from being attacked during the subsequent etching operation.

The device with attached leads is then etched, rinsed, vacuum baked at a high temperature and electrically tested. At this step, the device can be re-etched until the optimum electrical characteristics are attained. Once the device has been found to be electrically acceptable, it is coated to passivate the exposed silicon surface.

The encapsulation is described in Section III.

G. Electrical Evaluation

Figure 15 is a schematic of the test circuitry used to measure h_{FE}, $V_{CE(sat)}$, $V_{BE(sat)}$, t_d+t_r, and t_s+t_f.

$V_{CEO(sus)}$ and V_{ECO} were measured on a Tektronix Type 575 curve tracer.

The results were given in Table I.

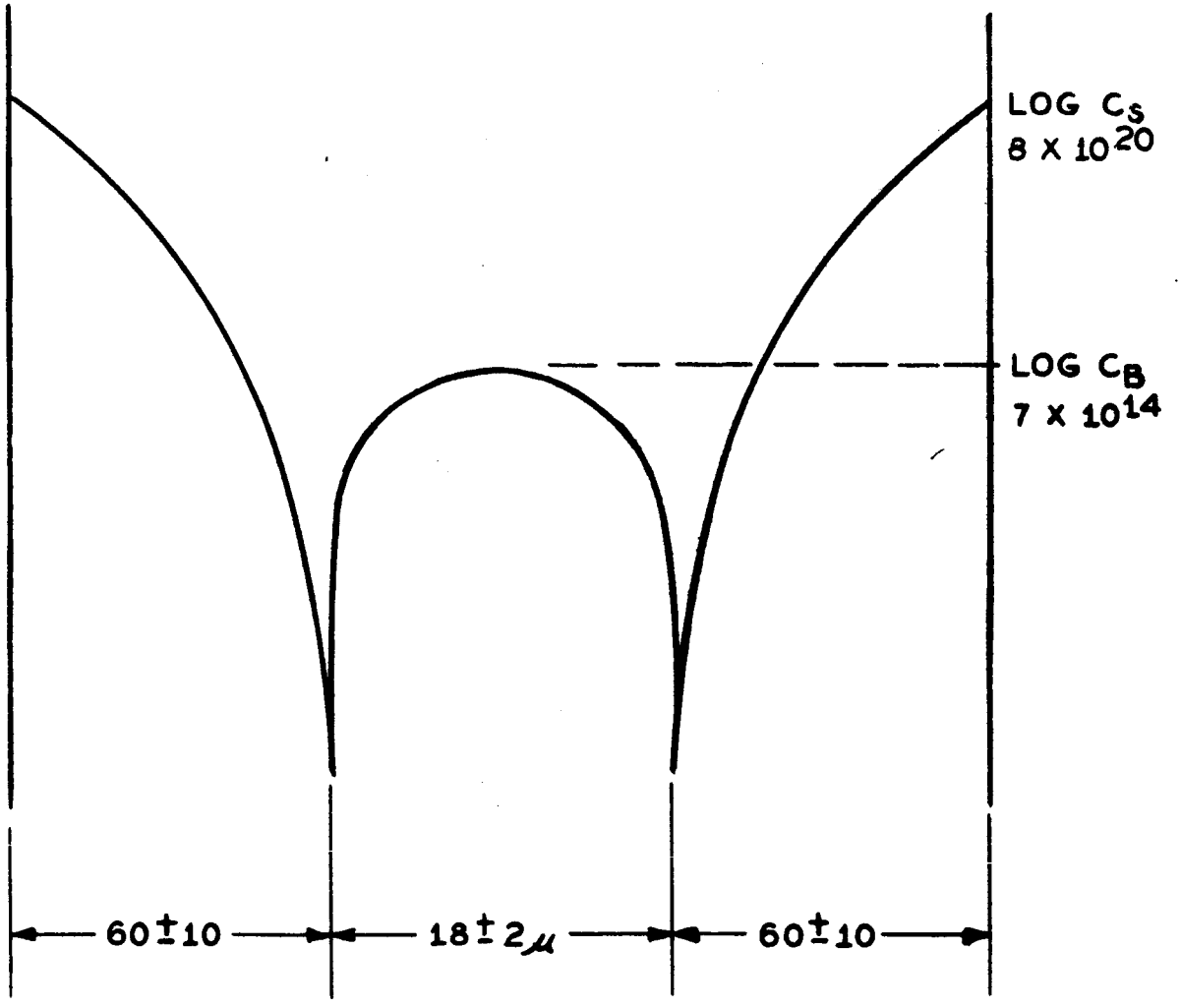


FIG. 5

VOLTAGE DESIGN

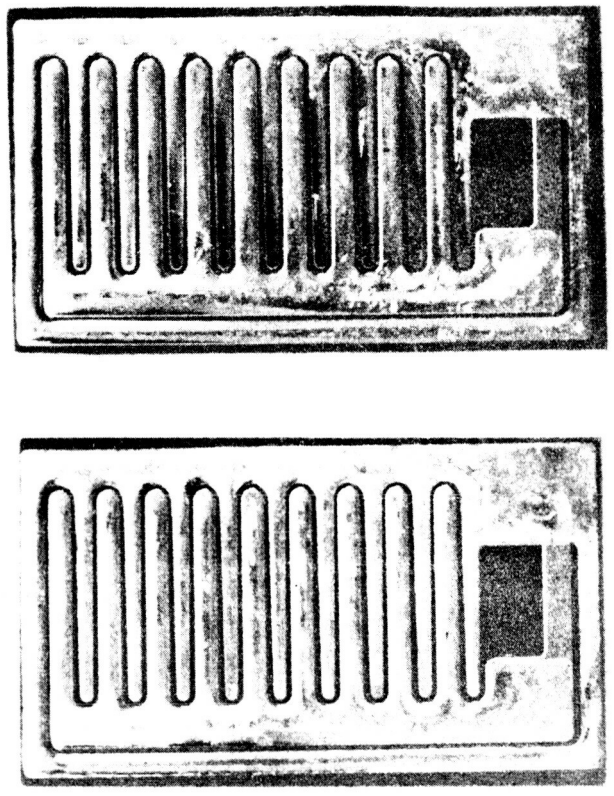


FIGURE 6

Integrated Transistor,
Resistor and Diode

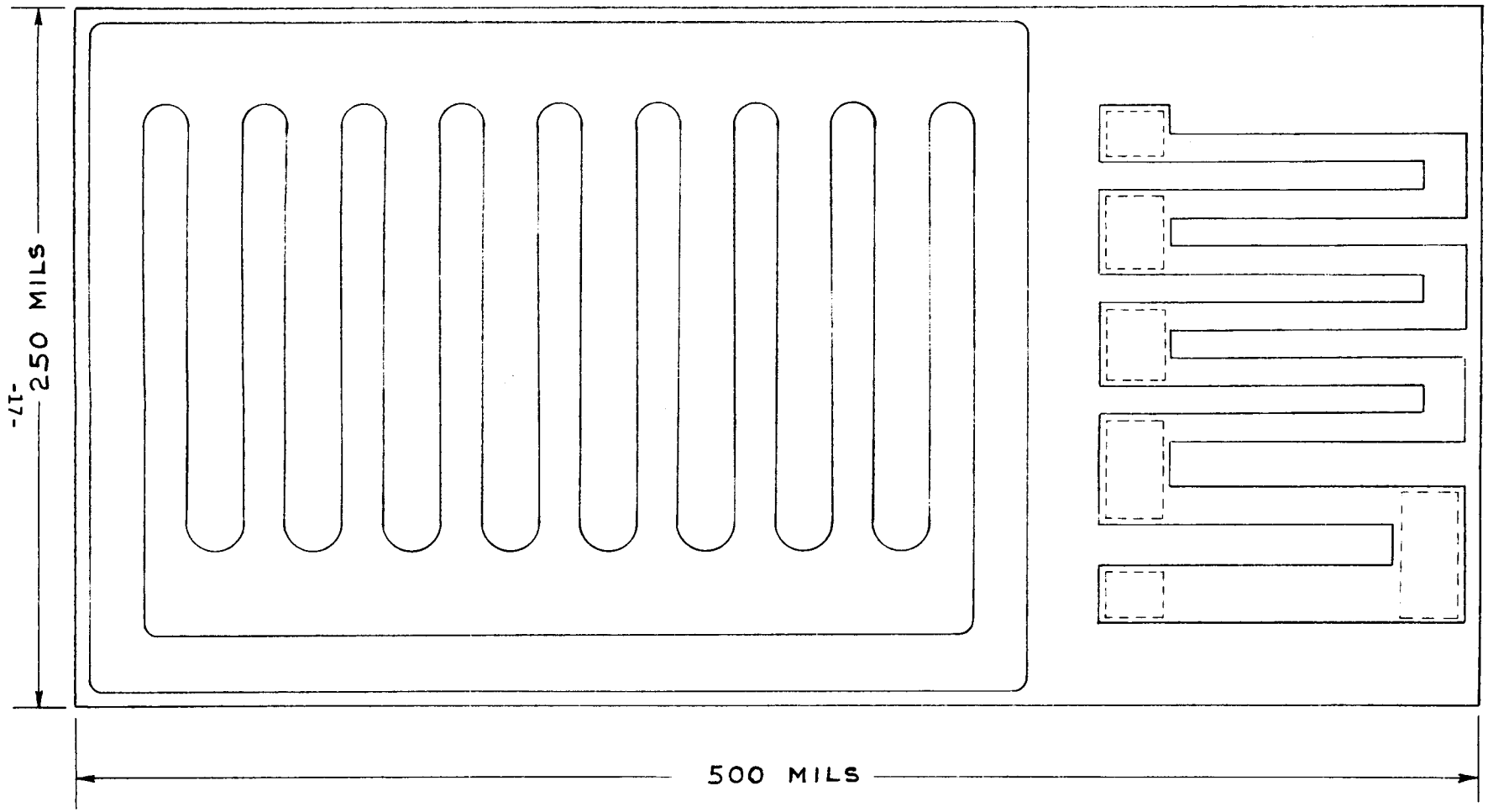


FIG. 7 - BASIC DEVICE GEOMETRY

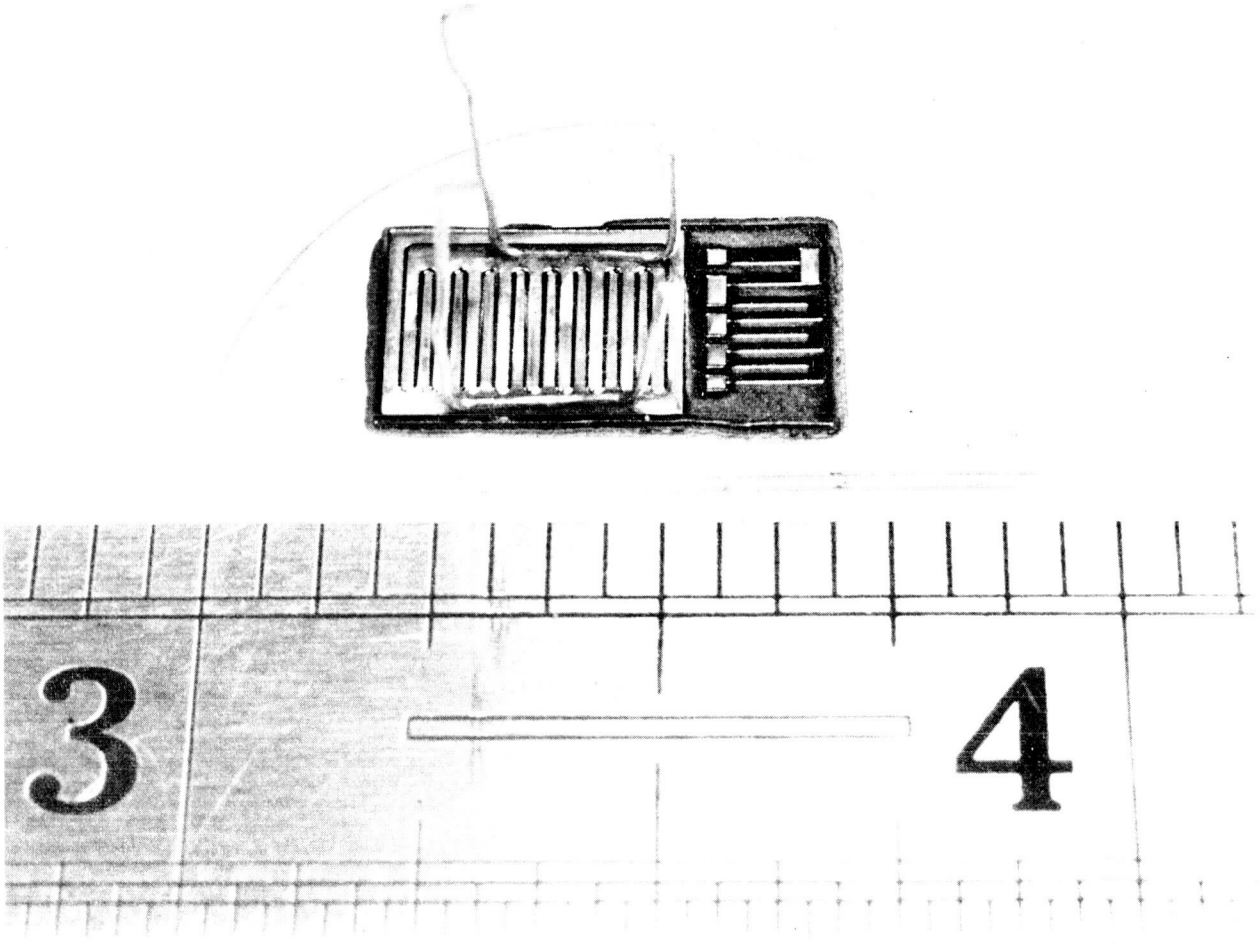


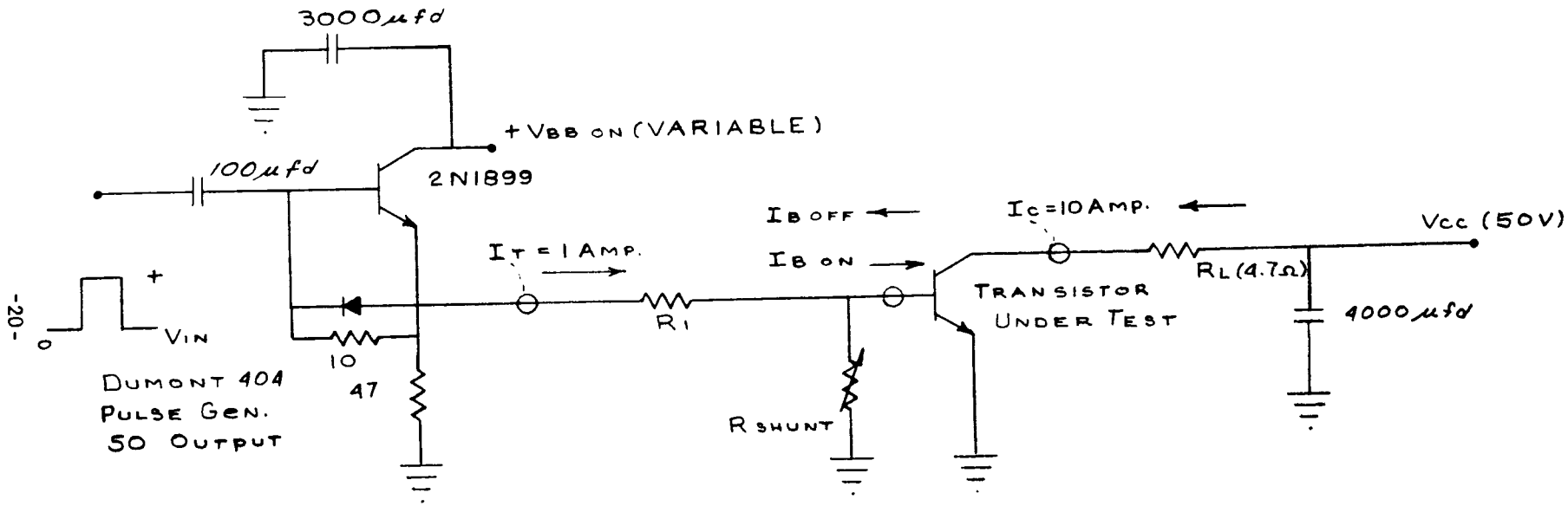
FIGURE 8

Basic Device Mounted on a
Molybdenum Platform (uncoated)

Table II

CHARACTERISTICS OF EXPERIMENTAL TRANSISTORS

	V_{EBO}	V_{CBO}	V_{CEO} 10 ma	V_{CEO} 20 ma	V_{CEX} 10	V_{CEX} 20	h_{FE} 5A	h_{FE} 10A	$V_{CE(SAT)}$ 5A	$V_{BE(SAT)}$ 5A	$V_{BE(SAT)}$ 10A	t_{D+P}	t_{S+F}
1	11.5V	130V	68V	80V	115V	125V	12.5	11.4	0.17V	0.82V	0.96V	1.8μsec	2.6μsec
2	12.5V	150V	105V	100V	120V	130V	29.6	18	0.18V	0.80V	0.96V	1.2μsec	2.6μsec
3	15.5V	130V	105V	100V	110V	125V	41.4	24.5	0.22V	0.90V	1.05V	1.4μsec	3.1μsec
4	10.5V	130V	105V	100V	105V	70V	73.6	34	0.13V	0.80V	0.90V	1.3μsec	5.4μsec



ALL CURRENTS MEASURED WITH
TEKTRONICS TYPE 131 CURRENT PROBE
WITH AMPLIFIER

FIG. 9 SWITCHING TEST CIRCUIT

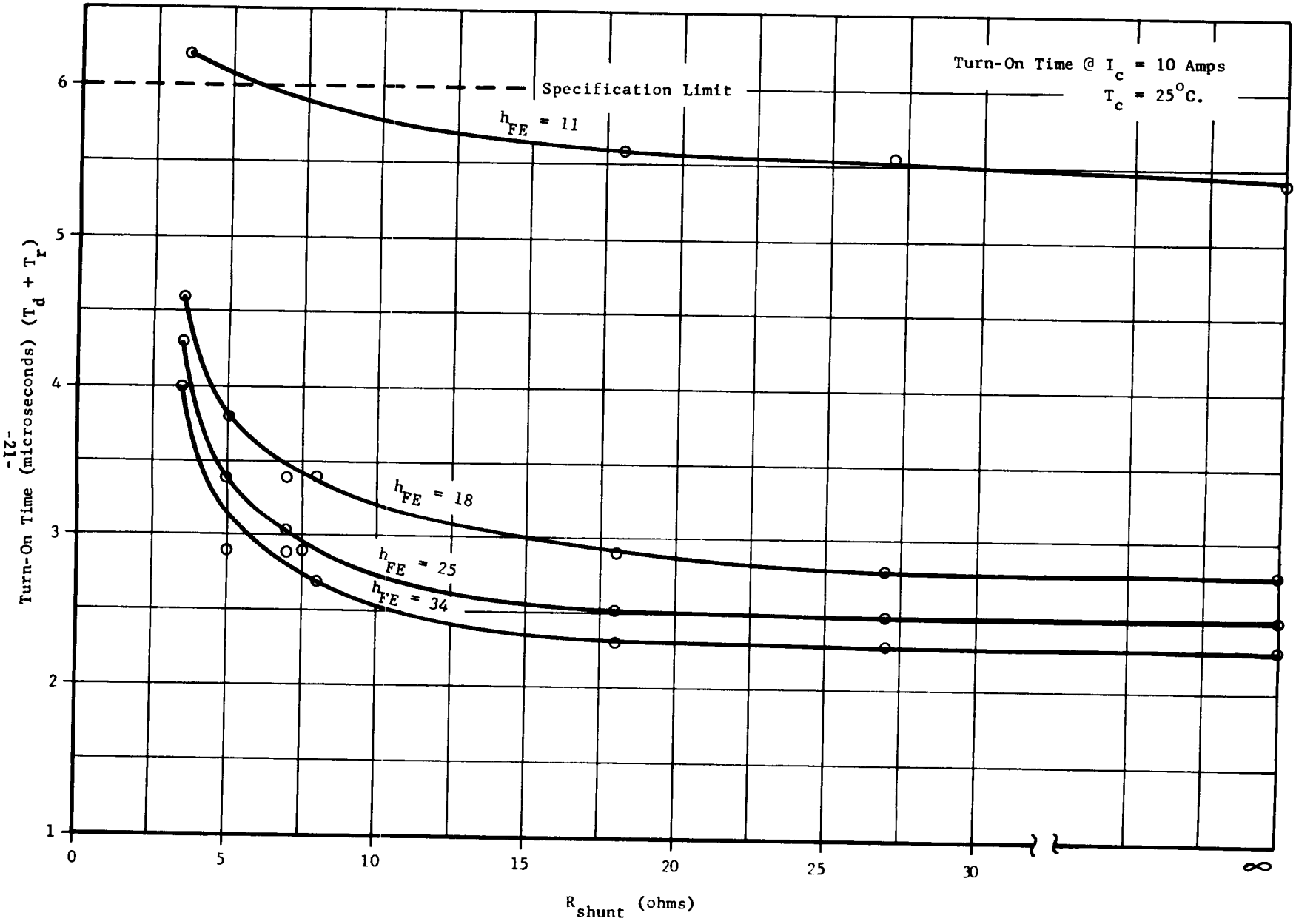


FIGURE 10 - TURN-ON TIMES OF EXPERIMENTAL TRANSISTORS

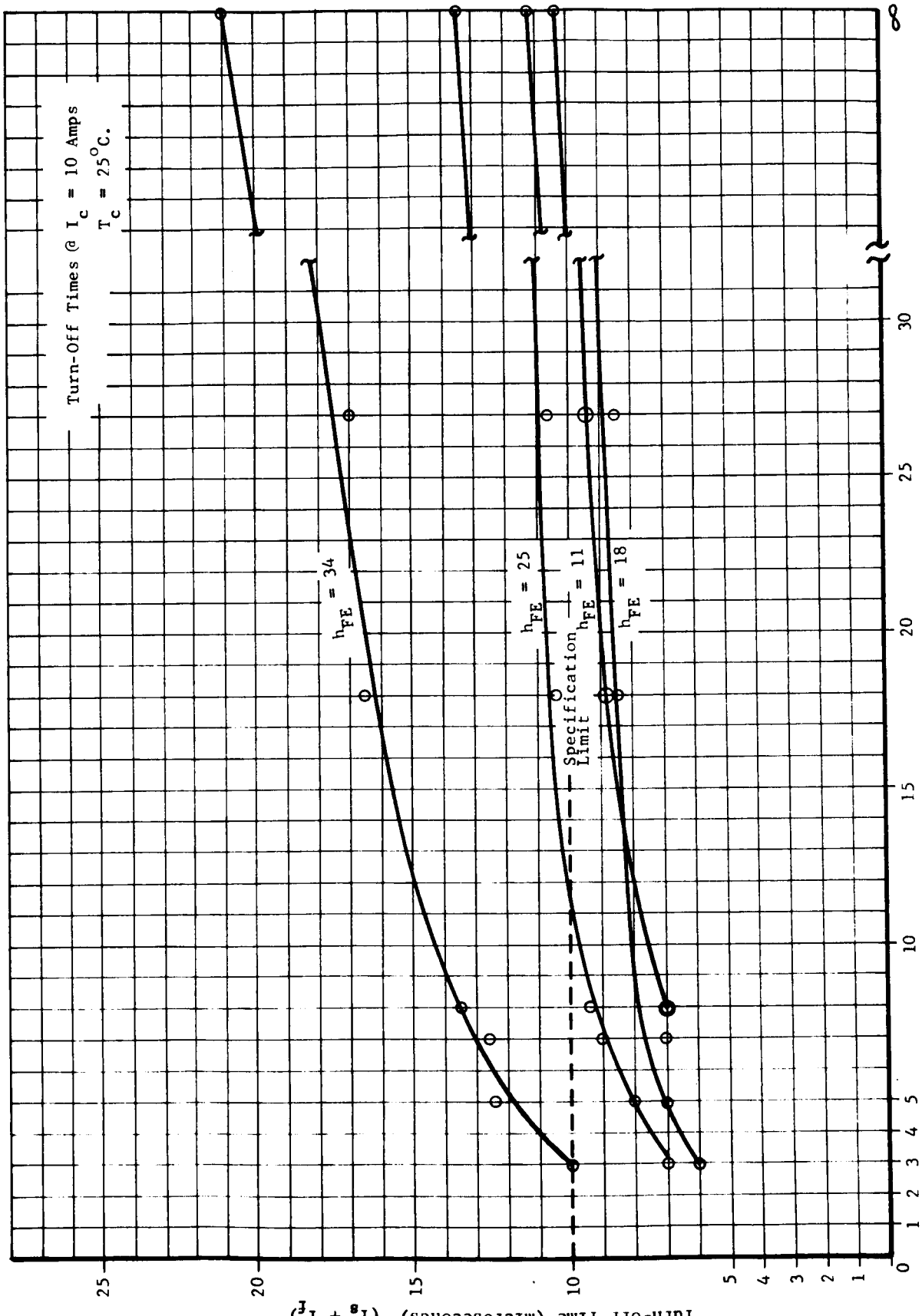
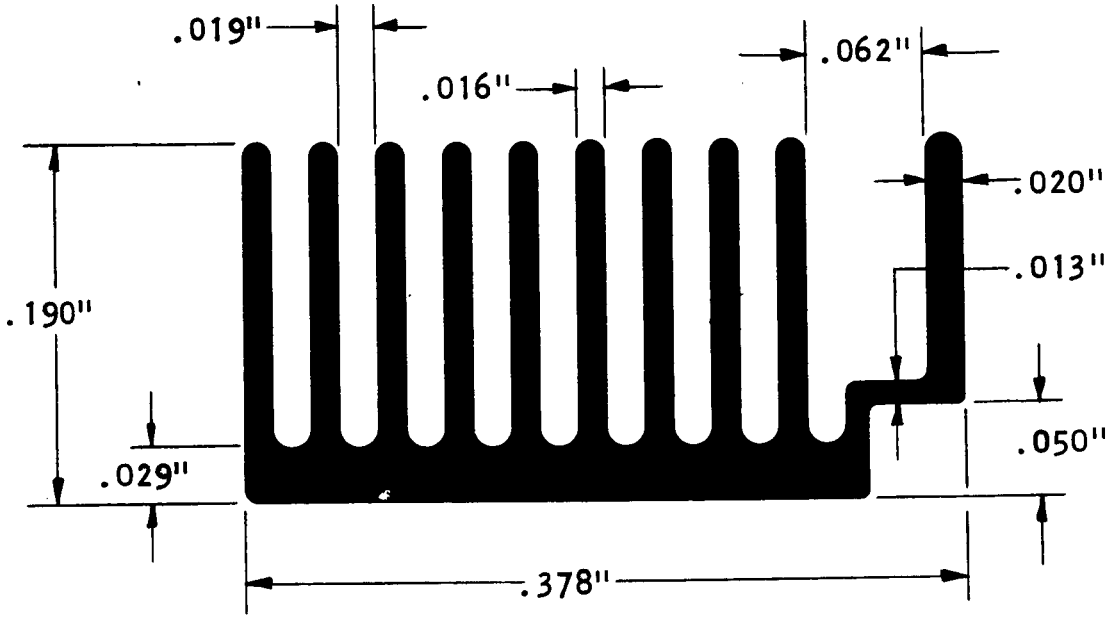


FIGURE 11 - TURN-OFF TIMES OF EXPERIMENTAL TRANSISTORS

TABLE III

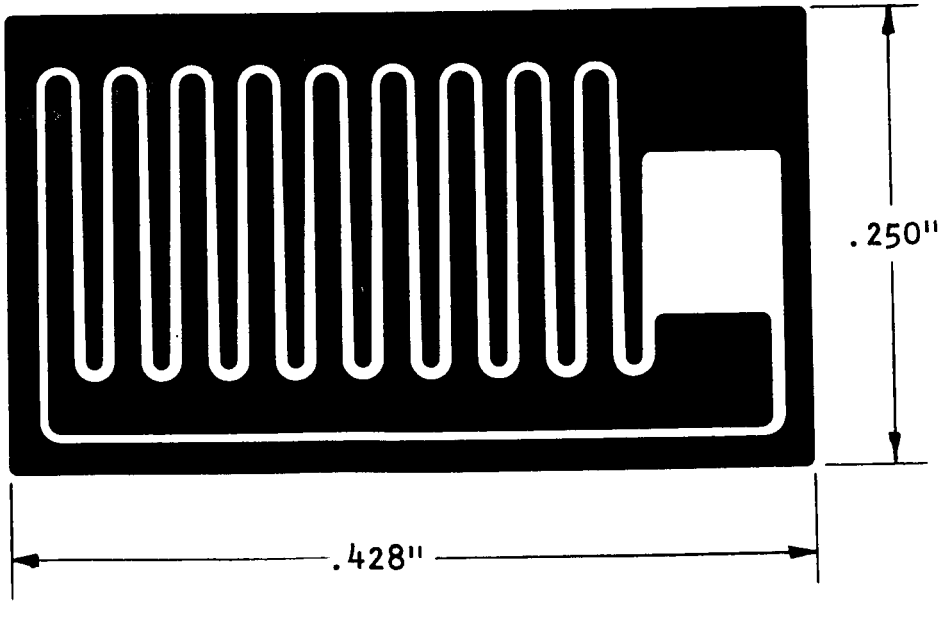
Switching Test Results

	A	B	C	D	E	F	G	H
Input Pulse								
cps rep. rate	8	8	8	8	8	8	8	8
μsec. pulse width	20	20	20	20	20	20	20	20
Transistor Test Conditions								
V_{cc}	6.0V	13	13	10	9.0	9.0	9.0	8.5
R_L	4.7ohm	4.7	4.7	2.7	1.4	1.4	1.4	1.4
I_c	1.0A	2.0	2.0	3.0	5.0	5.0	5.0	5.0
I_{B-on}	280ma	270	200	270	260	600	1.0A	1.0A
I_{B-off}	25ma	25	10	15	15	40	80	20
R_{on}	150ohm	150	150	150	150	68	22	22
R_{off}	68ohm	68	68	68	68	68	68	--
V_{BB-on}	50V	50	50	50	50	50	25	25
V_{BB-off}	3.7V	3.7	3.7	3.7	3.7	3.7	3.7	--
R_{EB}	17ohm	17	17	17	17	17	17	17
Switching Times								
τ_{delay}	0.4μsec.	0.4	0.5	0.5	0.5	0.5	0.4	0.4
τ_{rise}	0.9μsec.	0.85	3.5	3.1	5.9	2.0	1.6	1.6
Total τ_{on}	1.3μsec.	1.25	4.0	3.6	6.4	2.5	2.0	2.0
$\tau_{storage}$	1.9μsec.	1.5	0.9	1.2	0.8	1.8	2.8	3.4
τ_{fall}	1.3μsec.	1.8	1.8	2.3	3.1	3.0	3.2	4.6
Total τ_{off}	3.2μsec.	3.3	2.7	3.5	3.9	4.8	6.0	8.0



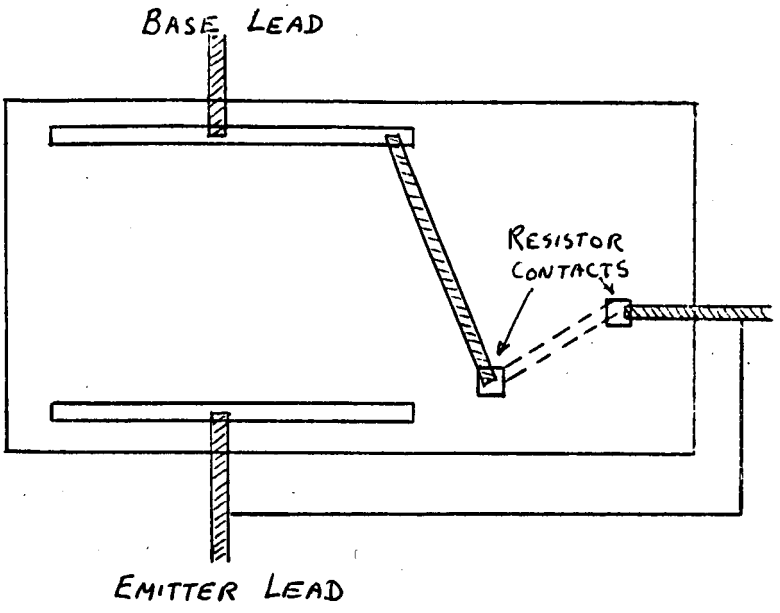
RESISTOR & EMITTER MASK

FIGURE 12(A)

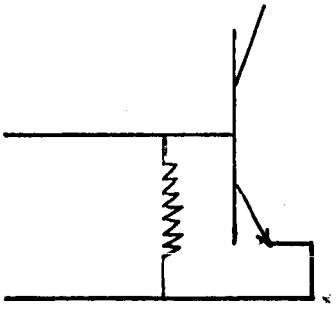


METALLIZING MASK

FIGURE 12(B)



PHYSICAL WIRING

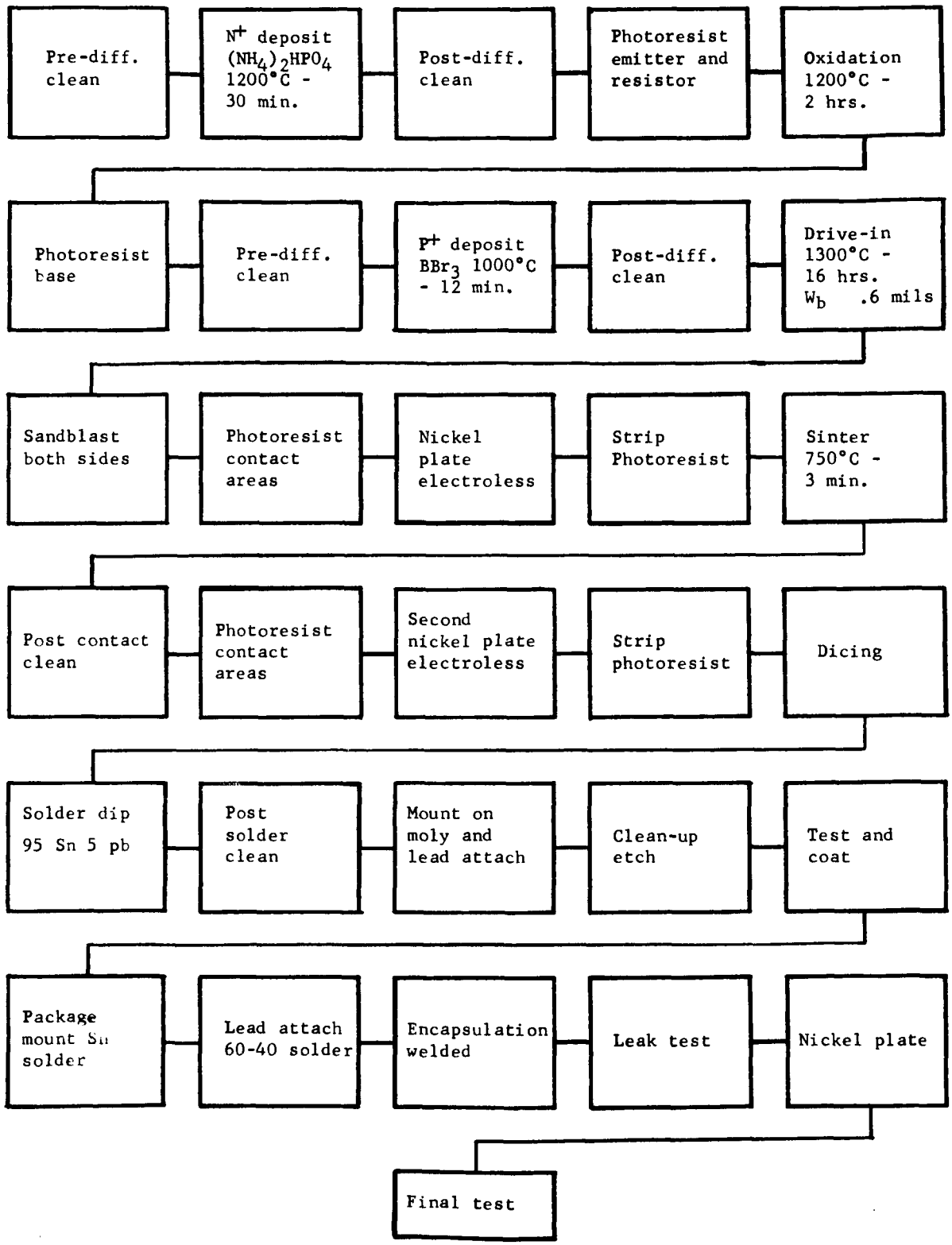


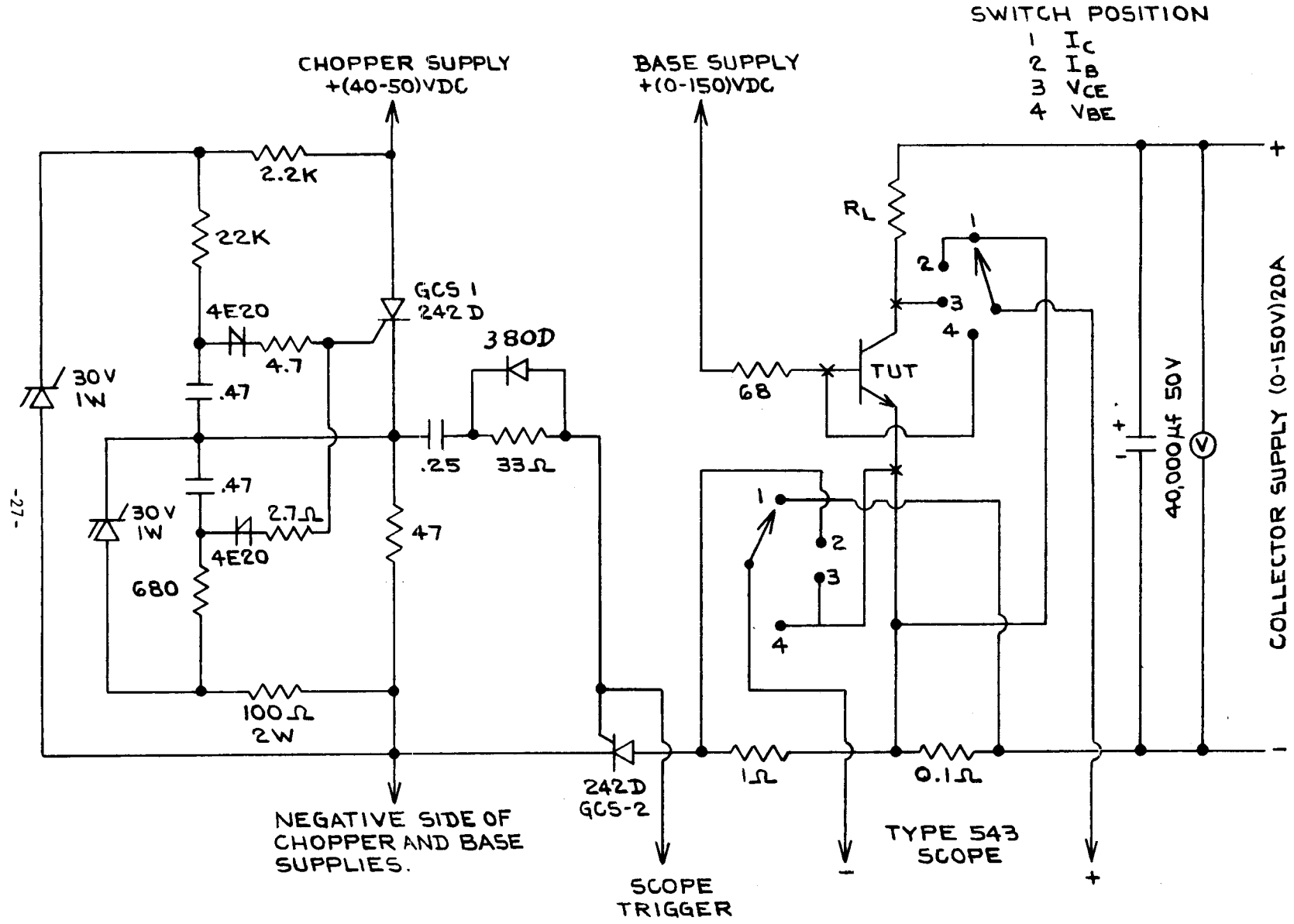
SCHEMATIC

FIG. 13

LEAD CONNECTION DIAGRAM

FIGURE 14: PROCESS FLOW CHART - SPLIT AMPLIFIER





SPLIT AMPLIFIER TEST CIRCUIT
FIG.15

III. ENCAPSULATION DESIGN

A. Specifications

The encapsulation package had to be designed to meet certain specifications, mechanical and environmental.

1. Mechanical:
   a. Hermetically sealed
   b. Device isolated from case
2. Environmental:
   a. Temperature cycle: -55°C to 125°C, 5 cycles
   b. Moisture resistance: 10 cycles
   c. Centrifugal: 500g --- 10,000g
   d. Shock: 500g
   e. Vibration: 20g, 100cps to 2000cps

B. Initial Design

The initial design concept was one of complete mechanical assembly. The encapsulated unit was designed to dissipate heat by conduction through an integral copper stud to a metal heat sink. In application, mounted units were not to be subjected to any direct contact with liquid or vapor cooling mediums. Following is a detailed explanation of each component of the encapsulation.

1. Basic Device:

The initial basic device (Figure 16) was a diffused silicon wafer with an overall dimension of .450 x .250 inches. Since the device was diffused, a means of contacting the wafer to another member was a problem. With the aid of photochemistry, selective areas (emitter and base) on one side of the wafer and the entire opposite (collector) side were electroless nickel plated. The nickel deposition was sintered into the silicon wafer in order to improve the chemical bonding between the nickel and silicon.

A second nickel plating operation followed; this was not sintered. Then each wafer was individually solder dipped; the solder adhering only to the nickel plated areas. This additional layer of metal served to conduct larger currents and aided the contacting of the internal emitter and base leads. Wafer bonding on the large collector area was also improved.

2. Molybdenum Semicircular Platforms:

The molybdenum platform designed and used to contact to the collector side of each device is shown in Figure 17. It was necessary to gold plate and sinter the molybdenum platform in order to protect it from any subsequent etching operations. The wafer is centrally located and soldered to the gold plated molybdenum platform. During the same operation, two internal silver lead wires, .012 inch in diameter, are soldered to the emitter and base terminals, respectively. All soldered connections are joined in a horizontal belt-type furnace using a hydrogen atmosphere. After soldering, the device is dip etched for several seconds in a (1:1:1) acid solution, rinsed in deionized water, vacuum baked and coated as shown in Figure 18.

3. Flat Base Design:

Figure 19 shows the basic design of the tellurium copper base which housed two of the processed wafers. Six holes were drilled into the base and threaded. A steel weld ring (Figure 20) was brazed to the copper and during the same operation a threaded stainless steel section was brazed into each hole. The brazed base assembly was silver plated in order to protect the copper from oxidizing and creating high thermal impedance paths.

4. Beryllia Discs:

A six-holed beryllia disc was manufactured as shown in Figure 21. The holes were drilled to clear the six stainless steel rods brazed into the base assembly. The purpose of this ceramic disc was to isolate the wafers from the base. Beryllia was chosen over many other ceramics because of its high thermal conductivity. Beryllia, 99.5% pure, possesses a resistivity of 1×10^{16} ohm-cm and a thermal conductivity of .63 cal/cm/cm^2/°C at room temperature. The thermal conductivity of beryllia at room temperature

is about 60% that of pure copper. Due to its high dielectric strength, good thermal conductivity and excellent thermal shock resistance, beryllia proved to be the best choice of the many available commercial ceramics.

5. Glass-Metal Seal:

Figure 22 shows a glass to metal seal which was used for encapsulation. Six tubular leads were isolated from one another with the use of colored glass. To help identify base, emitter and collector leads, three different colored glasses were used. The six silver internal leads are fed through their respective tubular leads and the flange of the seal is joined (by a resistance welding technique) to the weld ring brazed to the copper base. Figures 23 and 24 give a general outline of the encapsulated unit. The tubular leads are then pinch welded and pierced for final encapsulation. Protection against any corrosive atmosphere is attained by nickel plating the encapsulated unit and/or epoxy coating (see seal notes, Table IV).

6. Vertical Base Modification:

A modification in the base design became necessary when problems in brazing occurred. These arose when the threaded sections were brazed into the tapped holes of the flat base design. If insufficient braze material was used, the strength of the brazed joint was poor or inconsistent. On the other hand, if too much braze was used it would fill in the upper portion of the threaded section by capillary action and the nuts would not screw on. Therefore a vertical base as shown in Figure 25 was designed. For this design, only the weld ring was brazed to the copper base. The beryllia discs had to be cut in half in order to be used; and the number of screws and nuts were halved. The balance of the components, such as the molybdenum platform, the basic device, and the glass to metal seal remained unchanged.

7. Assembly:

The principle of assembly was essentially the same for both the flat and vertical base designs. After the devices were soldered to the molybdenum platform, etched, coated and electrically tested, two compatible devices

were selected for assembly. The devices required isolation from each other and from the base itself. To accomplish this end, a beryllia member was inserted between the copper base and the molybdenum platform. It was anticipated that contact resistance at each interface would create significant thermal resistance within the encapsulated unit. To reduce this contact resistance, a ductile material with good thermal conductivity characteristics was needed. Indium foil would have been the most suitable material except for one fault, its low melting temperature. Indium melts at 155°C and it was felt that this was too close to the specified maximum cycling temperature of 125°C. Therefore, silver foil was selected to be inserted at the copper-beryllia and beryllia-molybdenum interfaces. Small cylindrical shaped pieces of shrinkable teflon were placed around each threaded rod to insulate the stainless steel rod from the molybdenum platforms. Finally, the devices were in a position to be mechanically tightened in place with a stainless steel nut, Belleville washer, thrust washer and teflon washer. The Belleville washer was used to compensate for expansion and contraction of matching components during temperature cycling; and the purpose of the teflon washer was again for electrical insulation. Prior to final encapsulation the base assembly with the two mounted devices was vacuum baked along with a flexible fiberglass molecular sieve and the glass to metal seal. When the components are removed from the oven the seal is resistance welded to the base. Without removing the unit from the evacuated dry box, five of the six tubular leads are pinch welded. The unit is backfilled with helium through the last tubular lead and finally pinch welded. Small diameter holes are punched into the end of each lead and tests for hermeticity are run. If the unit shows a leak rate less than 10^{-5} cubic centimeters per second, it is removed and nickel plated. Nickel plating provides a final metal coating over all the bare and welded areas for protection against most environmental conditions. The transition from the initial flat base package to the vertical base package, with the major components, is shown in Figures 26 and 27.

C. BeO Metal Base Flat-Package Design

1. Metalization:

There is no universal metalization technique which is applicable to all ceramics. Techniques used to metalize commonly used ceramics such as alumina, Al_2O_3, have been successful for many years with a molybdenum-manganese (4:1) compound. These standard procedures could not be utilized with a hundred percent success on beryllia, BeO. The ratio of Mo-Mn had to be modified in the application of the slurry to the beryllia and the sintering temperature was reduced by 50°C in order to insure proper bonding to the ceramic. The metalizing process entailed either spraying or silk screening a Mo-Mn slurry onto an area of the beryllia and sintering at high temperatures in a reducing atmosphere. After sintering the Mo-Mn compound to the ceramic, the metalized area was copper plated for subsequent brazing operations. Beryllia was chosen over other ceramics because of its excellent thermal and dielectric characteristics. The thermal conductivity of beryllia (>99% pure) is comparable to aluminum (99.8% pure) from room temperature to 100°C. At higher temperature, such as 175°, beryllia is about 65% as efficient as aluminum. At all three temperatures the thermal conductivity of beryllia is at least eight times greater than alumina (99.5% pure).

2. BeO Metal Brazing:

The expansion coefficient of beryllia is the same as alumina; therefore, the same metals can be bonded to either by using the same technique. Kovar and high nickel-iron alloys are commonly used to bond ceramics. The brazing material which has proven to be successful is a silver-copper eutectic alloy which melts at 720°C. Brazing of metal to ceramic with this alloy is performed at 800°C in a hydrogen environment. The metal eyelet of the base assembly was brazed to the periphery of the beryllia disc and six copper core leads were brazed into six individually drilled and metalized holes. To insure hermeticity, a small kovar washer was brazed externally around each of the six protruding lead wires. The most difficult problem which occurred during the development of the base assembly was the copper stud to ceramic connection. The problem was twofold.

One was the difference between the expansion coefficients of beryllia and copper (1:2 1/2) and the other was the peeling of the metalized area caused by poor bonding between the metalization and the beryllia. Modification of the Mo-Mn ratio and adjustment of the sintering temperature corrected the bonding strength of the metalization to ceramic; and an increase in the thickness of the beryllia improved the strength of the brazed joint between the copper stud and ceramic. Although this type of brazed joint increases the thermal resistance by 25%, no serious consequence is observed in the final application of the unit.

3. Molecular Sieve:

The internal volume of the unit permitted little room for a standard pressed molecular sieve. With this in mind, two approaches were made to incorporate a molecular sieve within the package to absorb any undesired moisture which may work its way into the encapsulated unit.

One was to use a molecular sieve in powder form and the other was to use a standard flexible disc-shaped fiberglass form impregnated with zeolite -- the fiberglass proved to be the most practical. The powder was fine and tended to blow into the flange of the eyelet during the welding operation, thus creating a situation where complete hermeticity of the unit would be doubtful. The fiberglass occupied about 35% of the disc volume, the balance being occupied by zeolite. Prior to encapsulation the sieve was baked in a vacuum oven at 300°C for a day to make it moisture free. After bakeout, the sieve was placed between the device and metal dome (both of which were also baked out) and the unit was resistance welded in dry air where the dew point was held at 2ppm.

4. Metal Dome:

The metal dome was designed and machined as shown in Figure 28. Two important features were incorporated into the design. One is the weld projection and the other is the splash guard ring. The steel dome is resistance welded to the kovar flange of the eyelet with the use of the electrodes shown in Figure 29. The weld projection and a small portion of the flange are the only areas heated to the melting temperatures of

the metals. Upon cooling the metals alloy with one another, forming a completely hermetic bond between them. The purpose of the splash guard is to prevent any of the molten metal from splashing onto the device. The welding electrodes were designed to enter the metal dome on the flange prior to the resistance welding cycle. After welding, the unit is leak tested and nickel plated. This final design is shown, along with its major components, in Figure 4.

D. Environmental Testing

A sample of encapsulated units was subjected to standard vibration, shock, centrifugal, temperature cycling and moisture resistance tests. Each unit was tested under all of the above conditions. After each test electrical data and leak ratios were obtained. Results showed that the units could survive these environmental tests both electrically and mechanically. Leak rate tests showed that the resistance welding of the metal dome to the eyelet was not inferior; and the brazed joint between the copper stud and beryllia withstood all tests. Failure of several external flexible leads showed that these leads should be designed as short as possible. Excessive handling and bonding of the leads also may have contributed to their failure. Electrical data also showed the ruggedness of the base assembly in its ability to protect the internal connections of both devices in each encapsulated unit.

Since the fulfillment of this contract consisted of a relatively small number of units, no extensive statistical data could be obtained from these environmental tests. Although these tests represented typical environmental conditions conducted on standard products by the Quality Assurance Group, additional samples would have to be tested in order to establish meaningful failure rates at a high confidence level for production units.

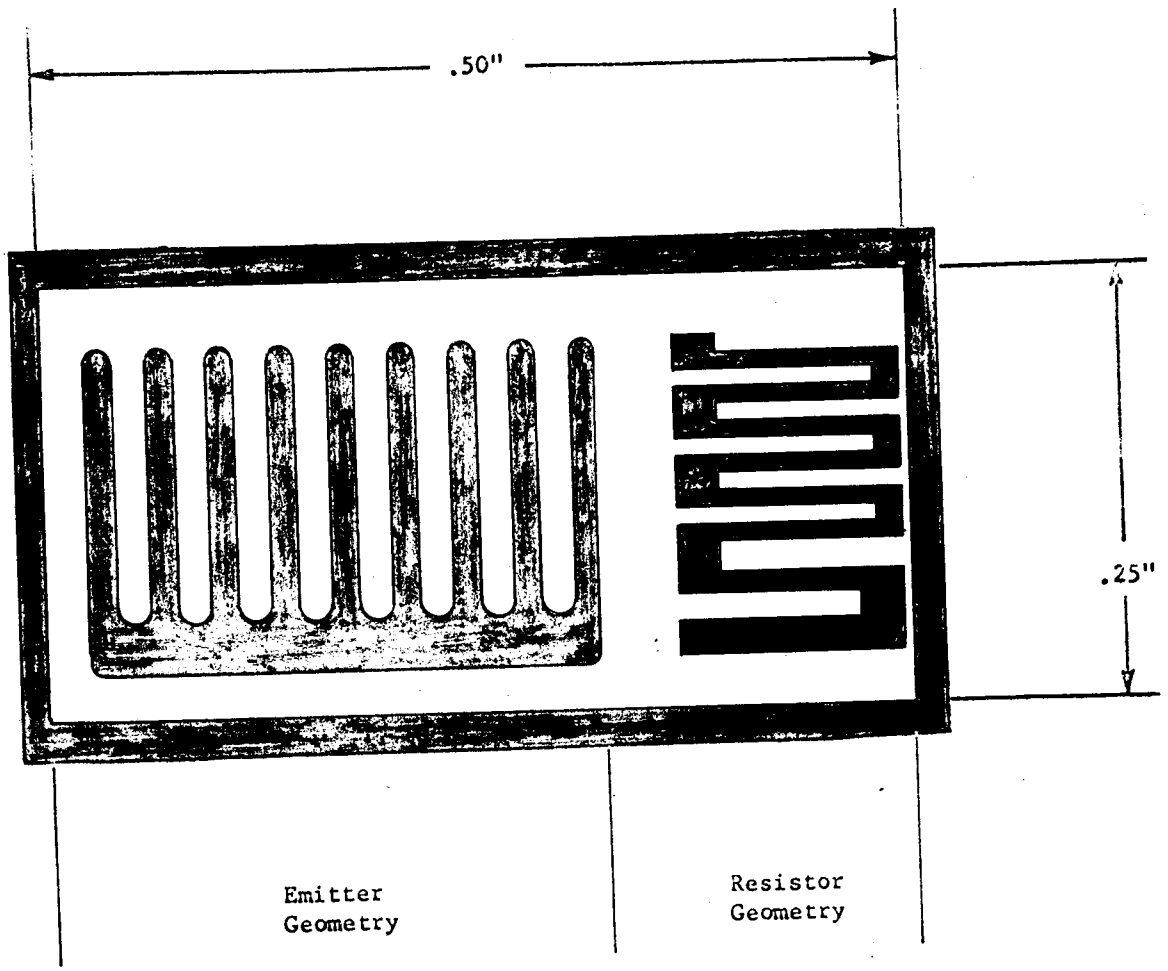


Figure 16 Emitter and Resistor Mask (Mesa Mask)
Scale 10:1

Moly Mounting for Integrated Power Amplifier

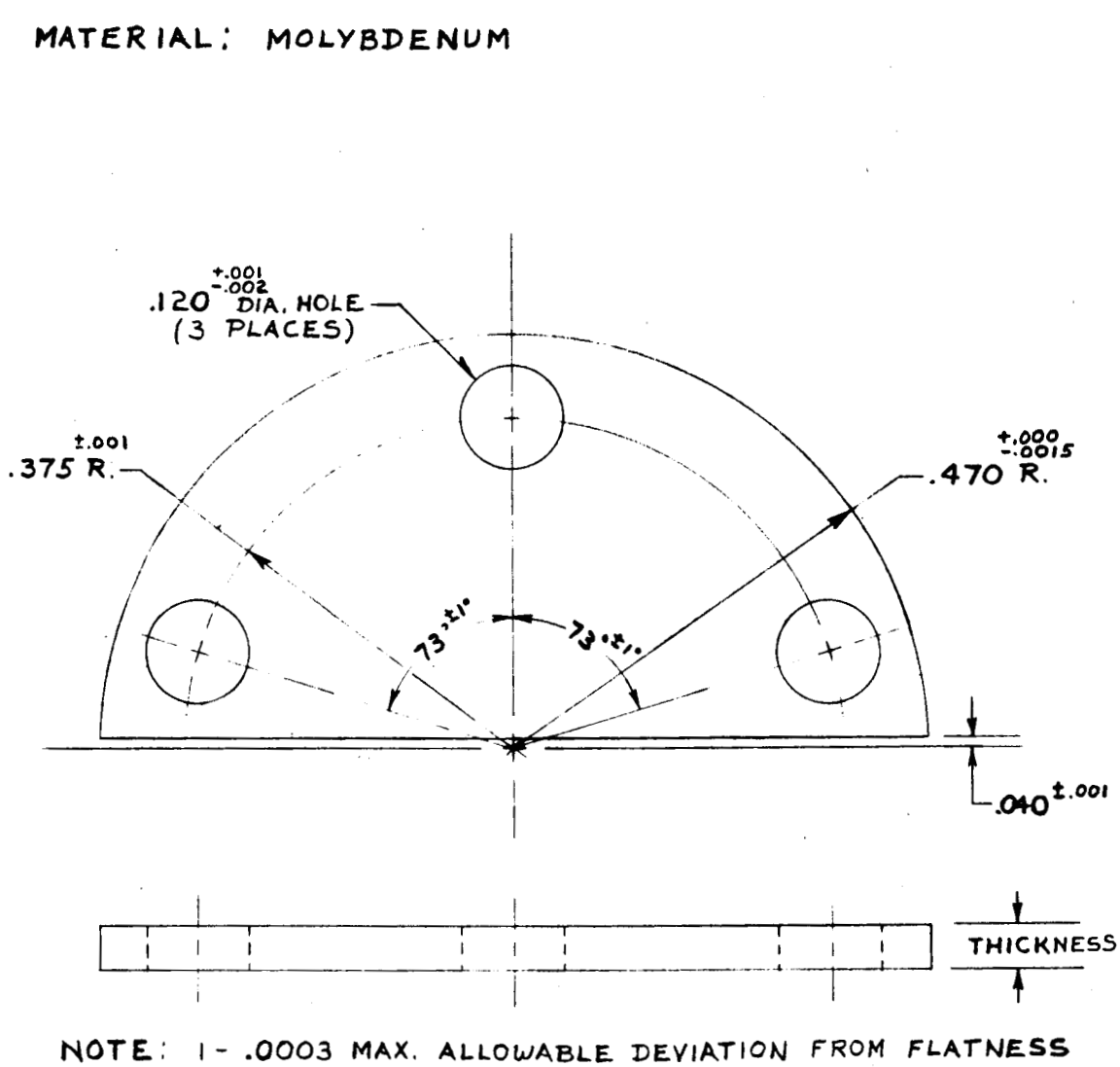


FIGURE 17: Molybdenum Platform

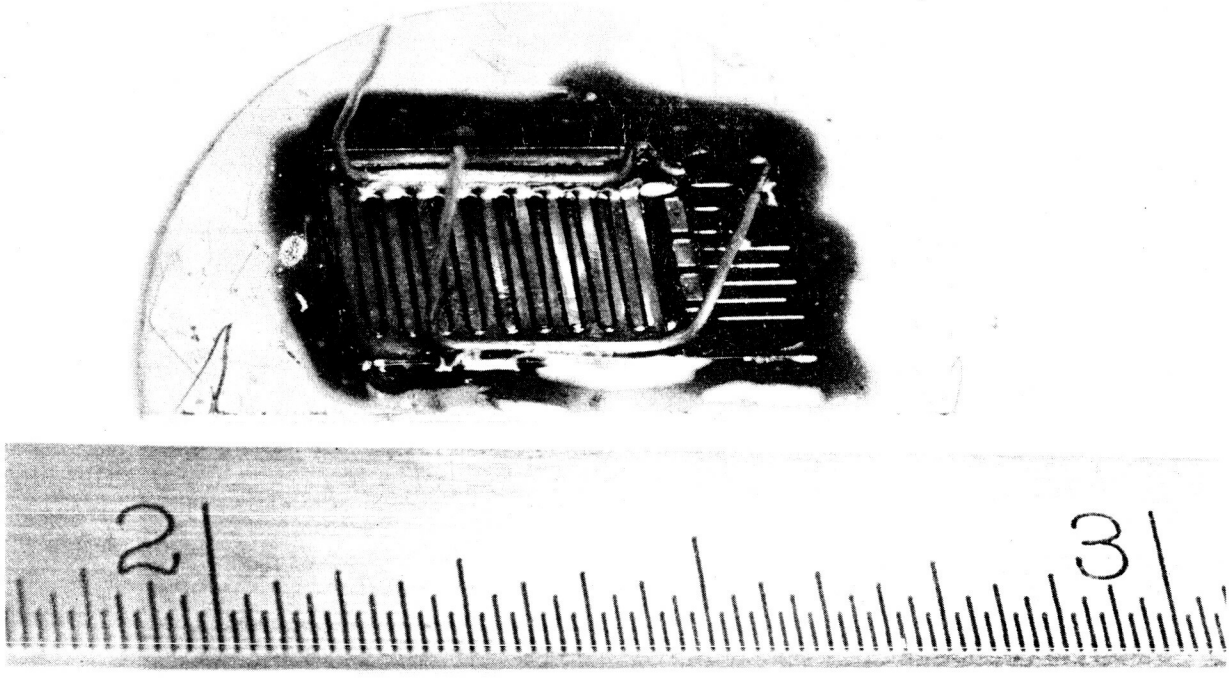
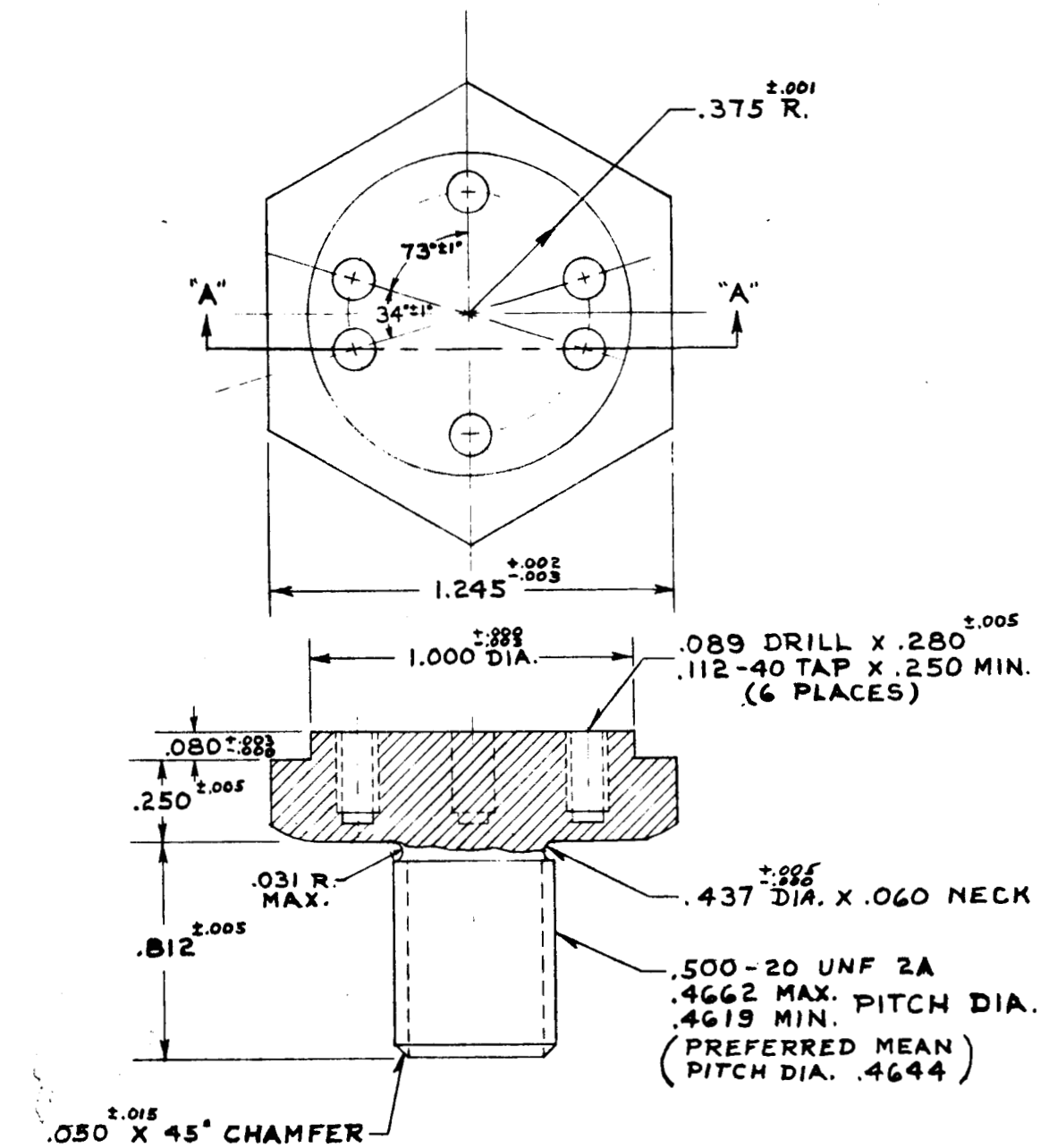


FIGURE 18

Basic Deviced Mounted
on a Molybdenum Platform
(coated)

Flat Mounting Base for Integrated Power Amplifier

MATERIAL: TE-CU



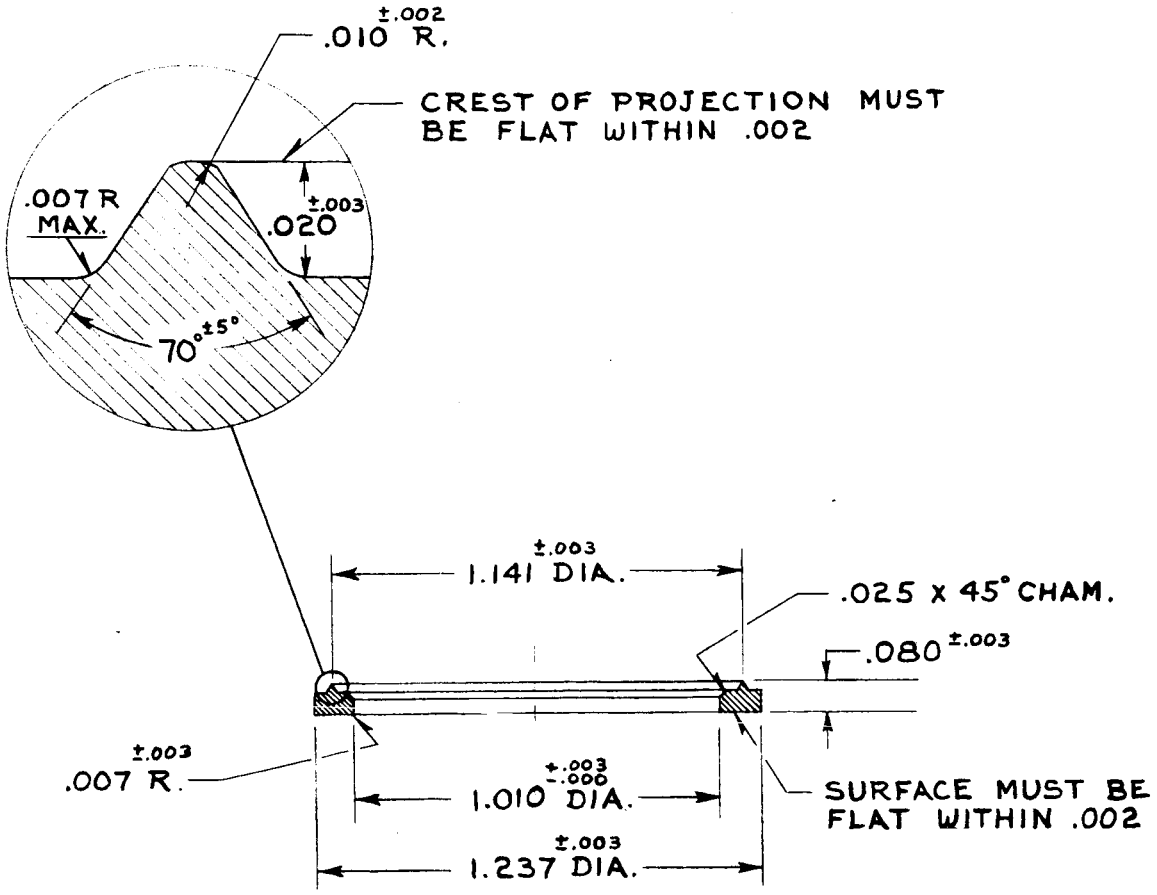
NOTE:

1- TAPPED HOLES TO BE PERPENDICULAR TO TOP SURFACE OF PEDESTAL WITHIN ½°.
2- PEDESTAL & SEATING PLANE MUST BE PARALLEL WITHIN .0005
3- PEDESTAL MUST BE FLAT WITHIN .0003
4- SURFACE FINISH OF PEDESTAL MUST NOT EXCEED 16/63
ALL OTHER MACHINED SURFACES NOT TO EXCEED

FIGURE 19: Flat Base (tellurium copper) Design

Weld Ring for Integrated Power Amplifier

MATERIAL: SAE 1008-1010 C.R. STEEL - P.D.S. 1689-1

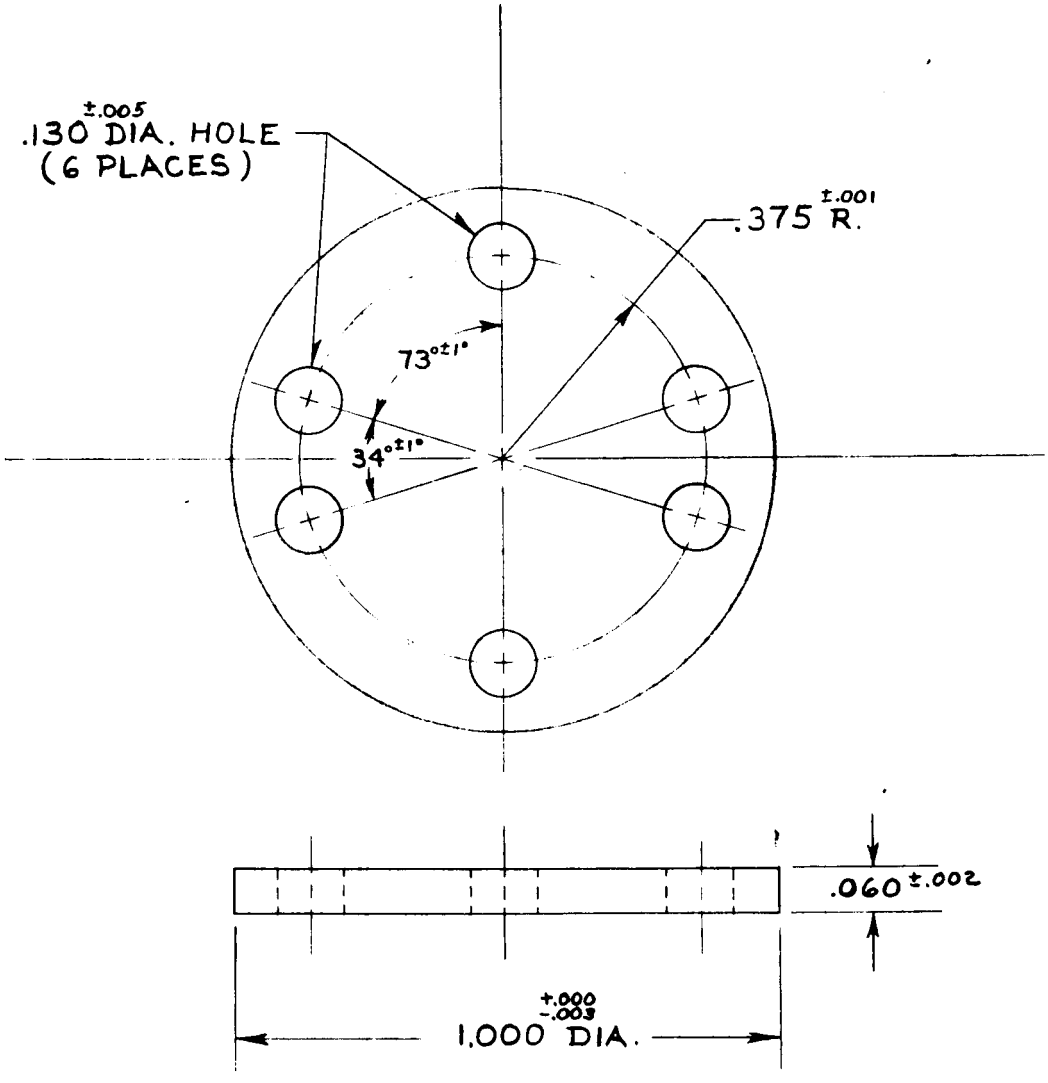


NOTE:
1- REMOVE ALL BURRS
2- ECCENTRICITY OF OTHER DIAMETERS TO I.D. MUST NOT EXCEED .006 T.I.R.

FIGURE 20: Steel Weld Ring

Ceramic Insulator for the Integrated Power Amplifier

MATERIAL: BERYLLIA CERAMIC



NOTE: 1 - .0003 MAX. ALLOWABLE DEVIATION FROM FLATNESS.

FIGURE 21: Beryllia Disc

G-M Seal for the Integrated Power Amplifier

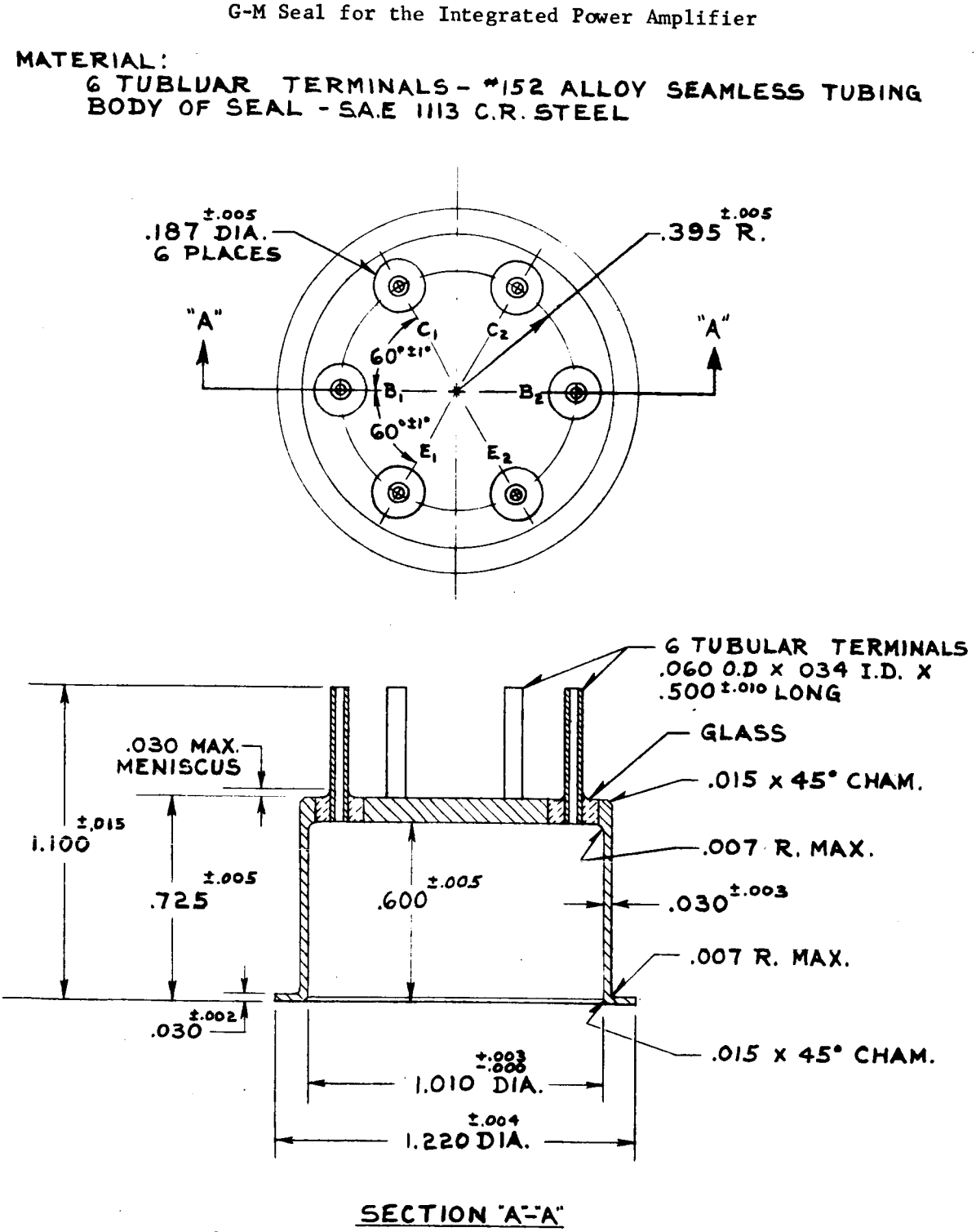


FIGURE 22: Glass-Metal Seal

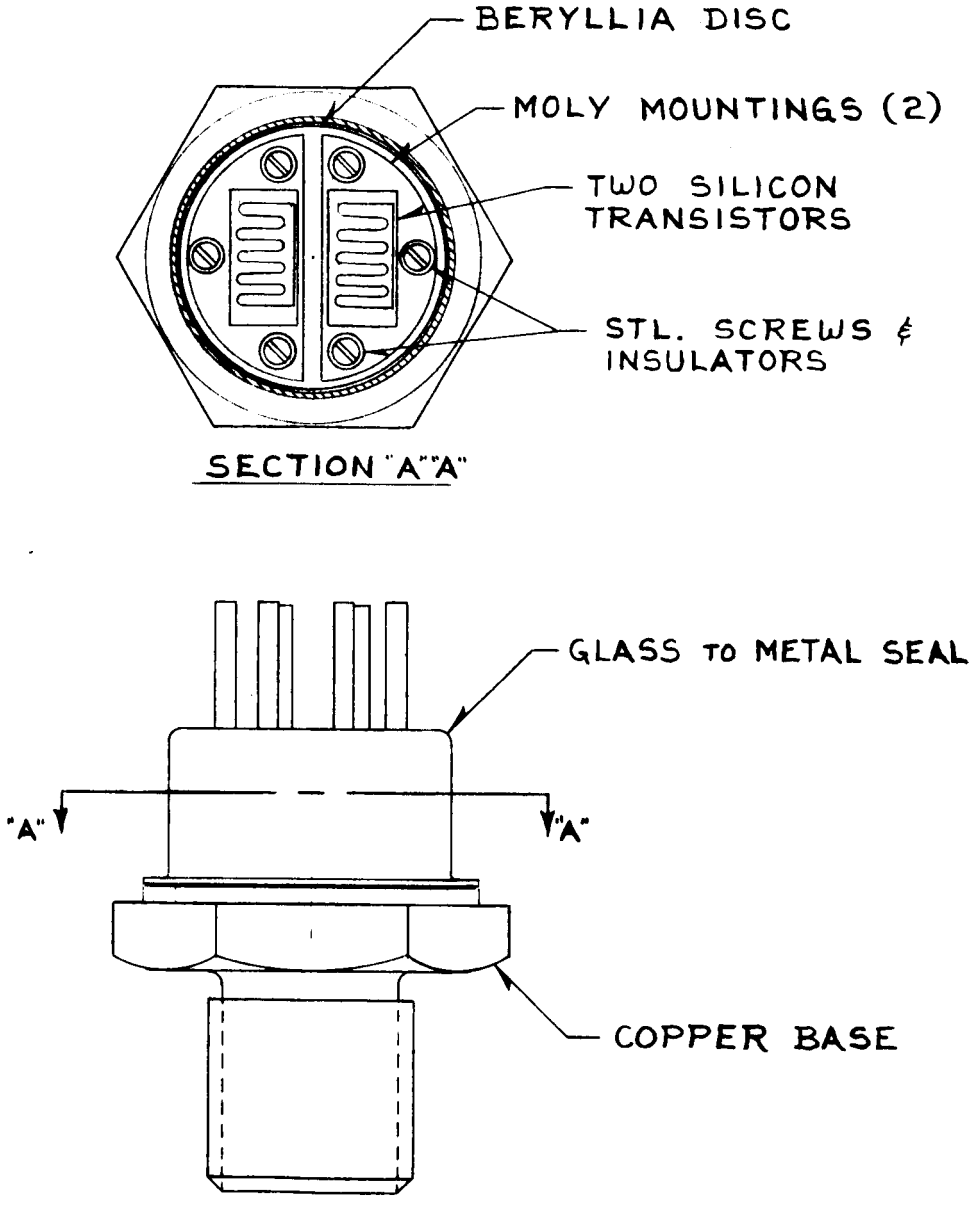


FIGURE 23: Integrated Power Amplifier - Encapsulation

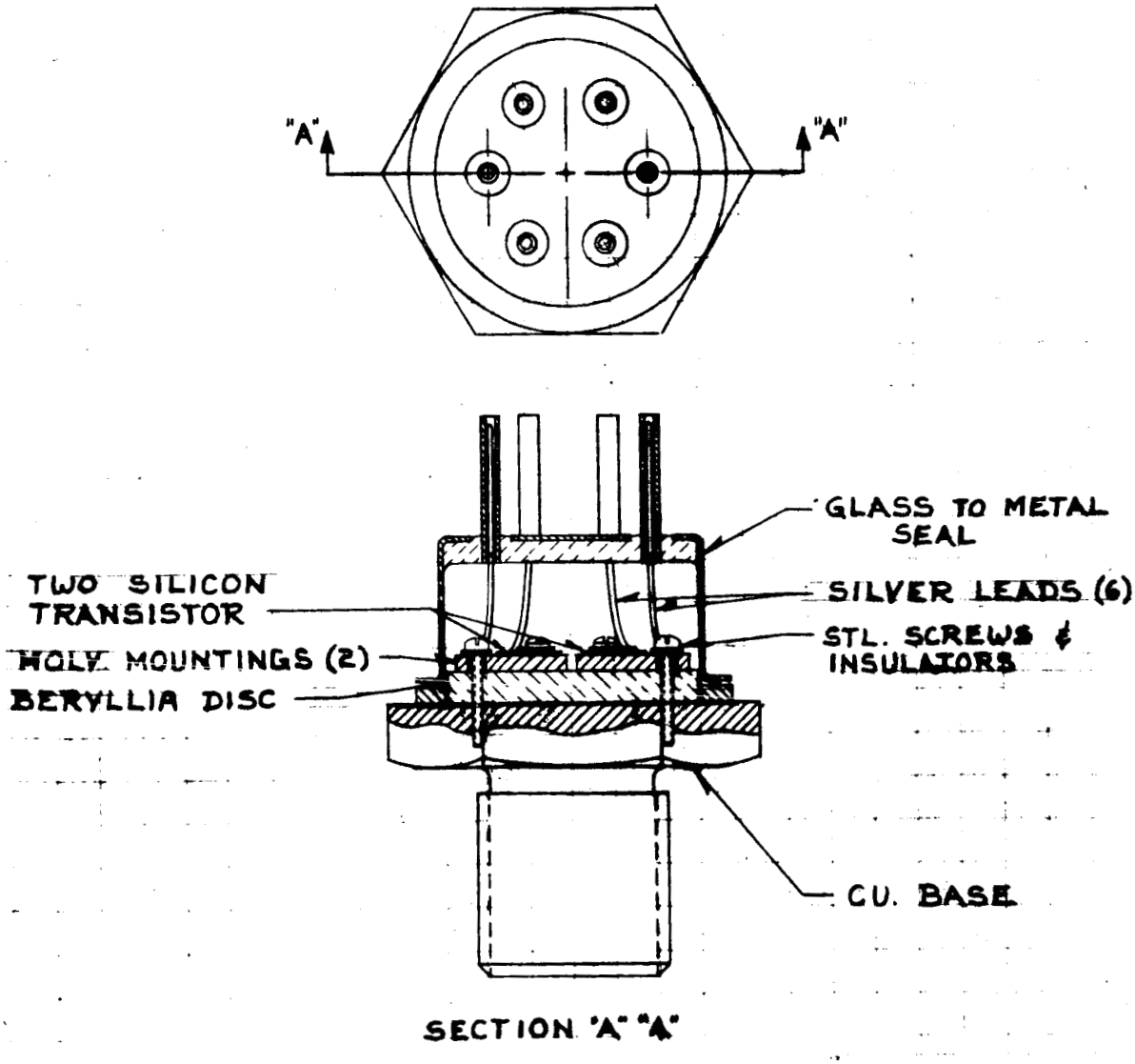


FIGURE 24: Integrated Power Amplifier - Encapsulation (cent.)

TABLE IV

SEAL NOTES (FOR INTEGRATED POWER AMPLIFIER)

GENERAL NOTES:

1. Seal must meet T. S. 710367.
2. Remove all burrs.
3. Flange surfaces must be individually flat within .002 and mutually parallel within .002.
4. Diameters must be concentric within .005 T. I. R.
5. Glass to be colored as follows:
   a. Red or brown for both collector terminals (C_1 and C_2)
   b. Blue for both base terminals (B_1 and B_2)
   c. Black for both emitter terminals (E_1 and E_2)

TERMINAL NOTES:

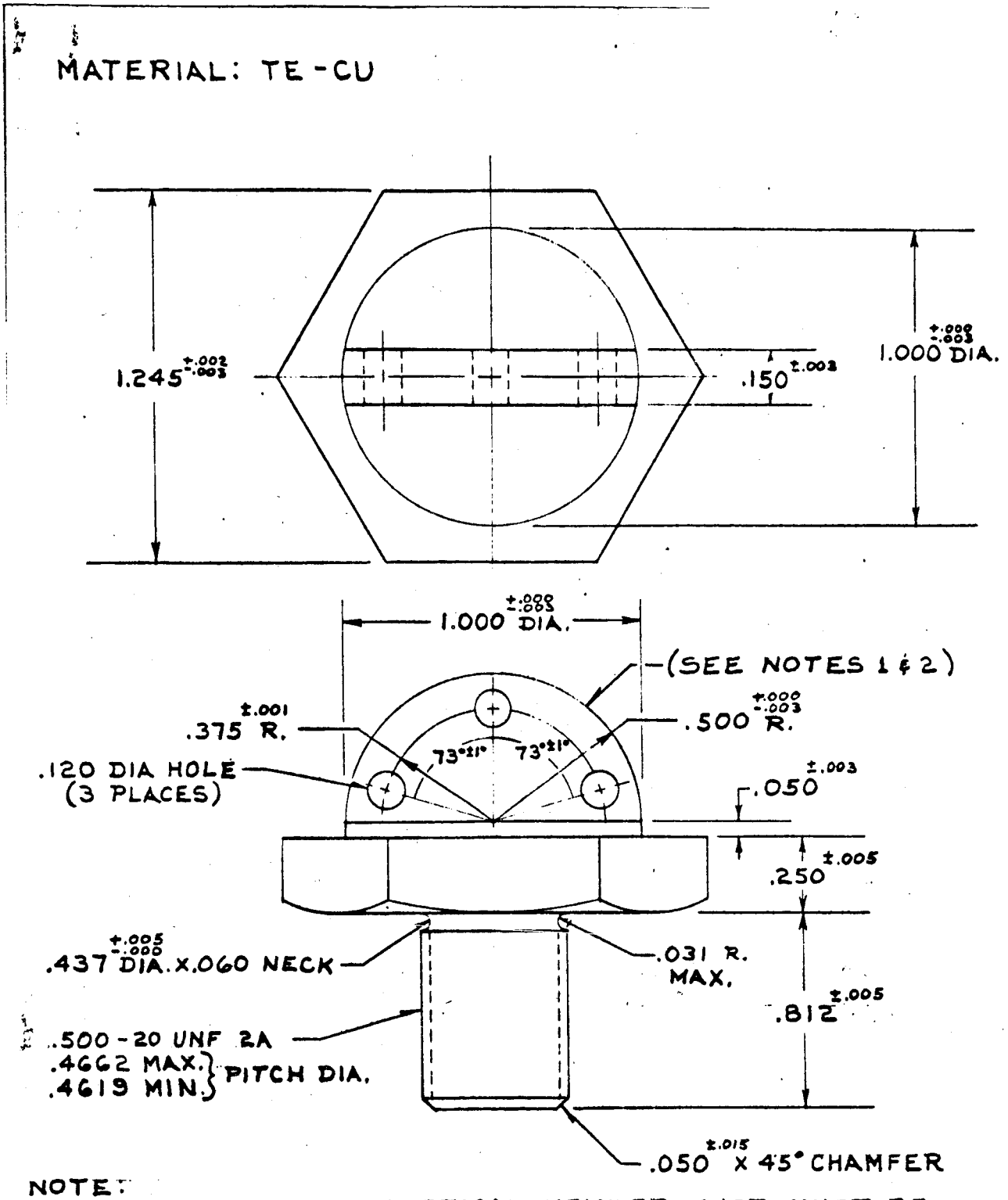
1. All terminals must be perpendicular to flange within 2^{o}.
2. Lower terminal ends and glass to be flush with top of internal cavity of seal body within .005.
3. Creepage path across glass between terminal tubes and body of seal must not be less than .055.

QUALITY NOTES:

1. Maximum allowable leak rate through seal joints, 10^{-8} cc/sec with differential pressure of 14.5 P.S.I.

FINISH NOTES:

1. 63 or better outside surface 83 on inside surface.
2. Apply copper flash 22AA05 (.0005 thick).



NOTE:
1- BOTH SIDES OF VERTICAL MEMBER MUST MUST BE PARALLEL TO EACH OTHER WITHIN .001 AND FLAT WITHIN .0003.
2- SURFACE FINISH OF VERTICAL MEMBER MUST NOT EXCEED 16, ALL OTHER MACHINED SURFACES MUST NOT EXCEED 63.

FIGURE 25: Vertical Base Design

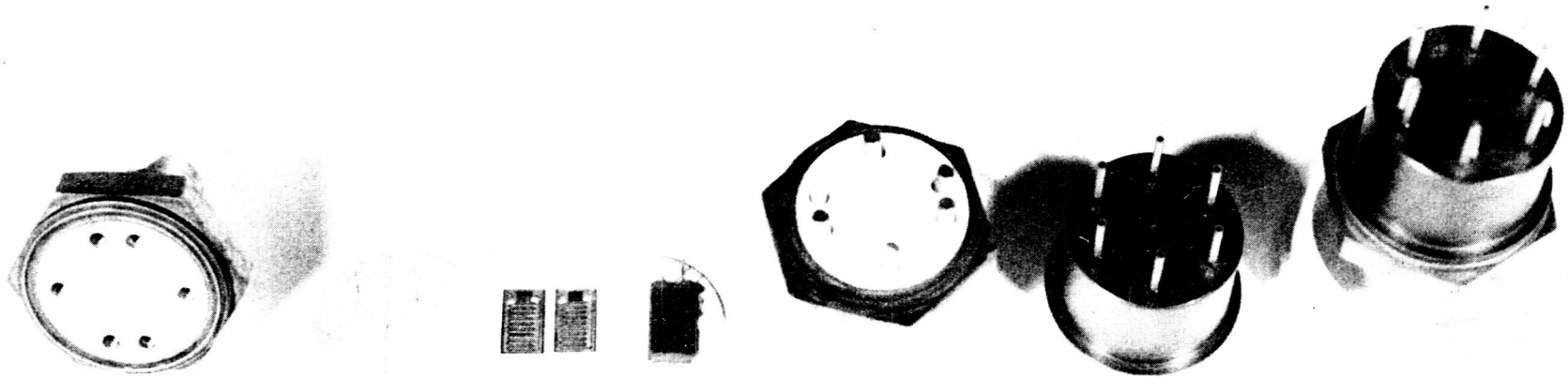


FIGURE 26

Flat Base Design
(with components)

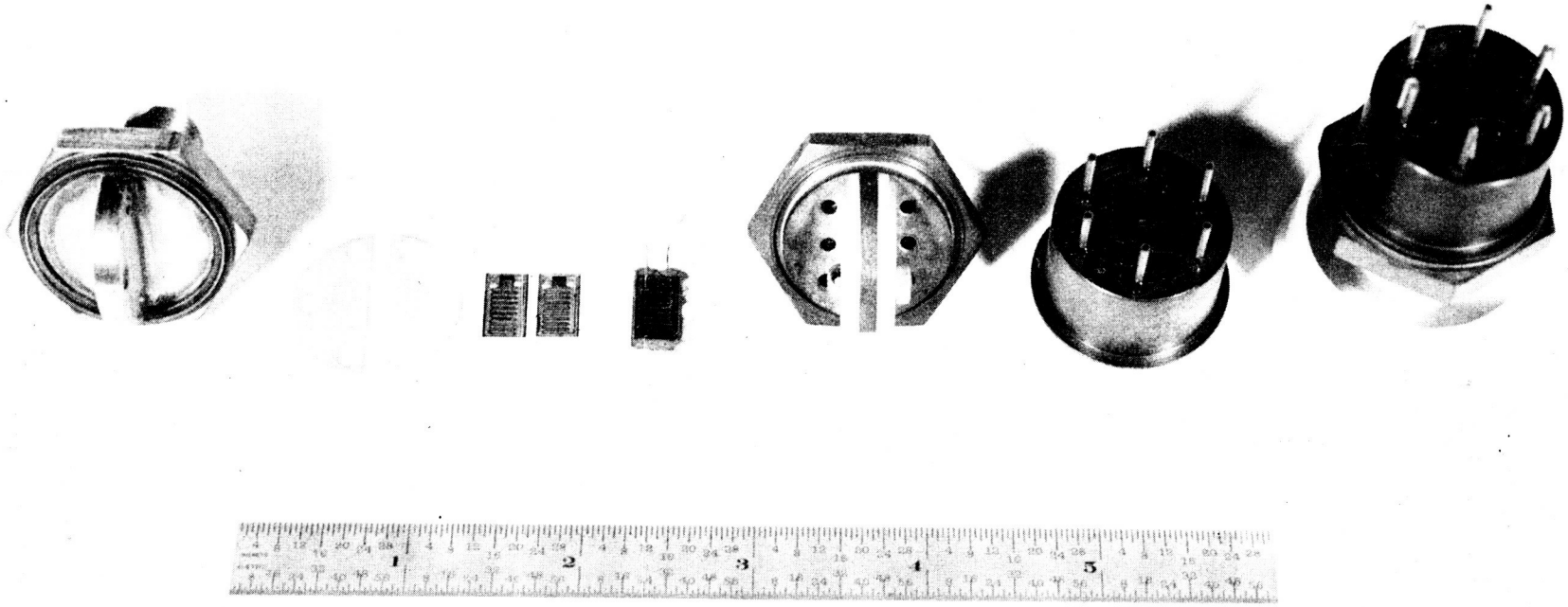
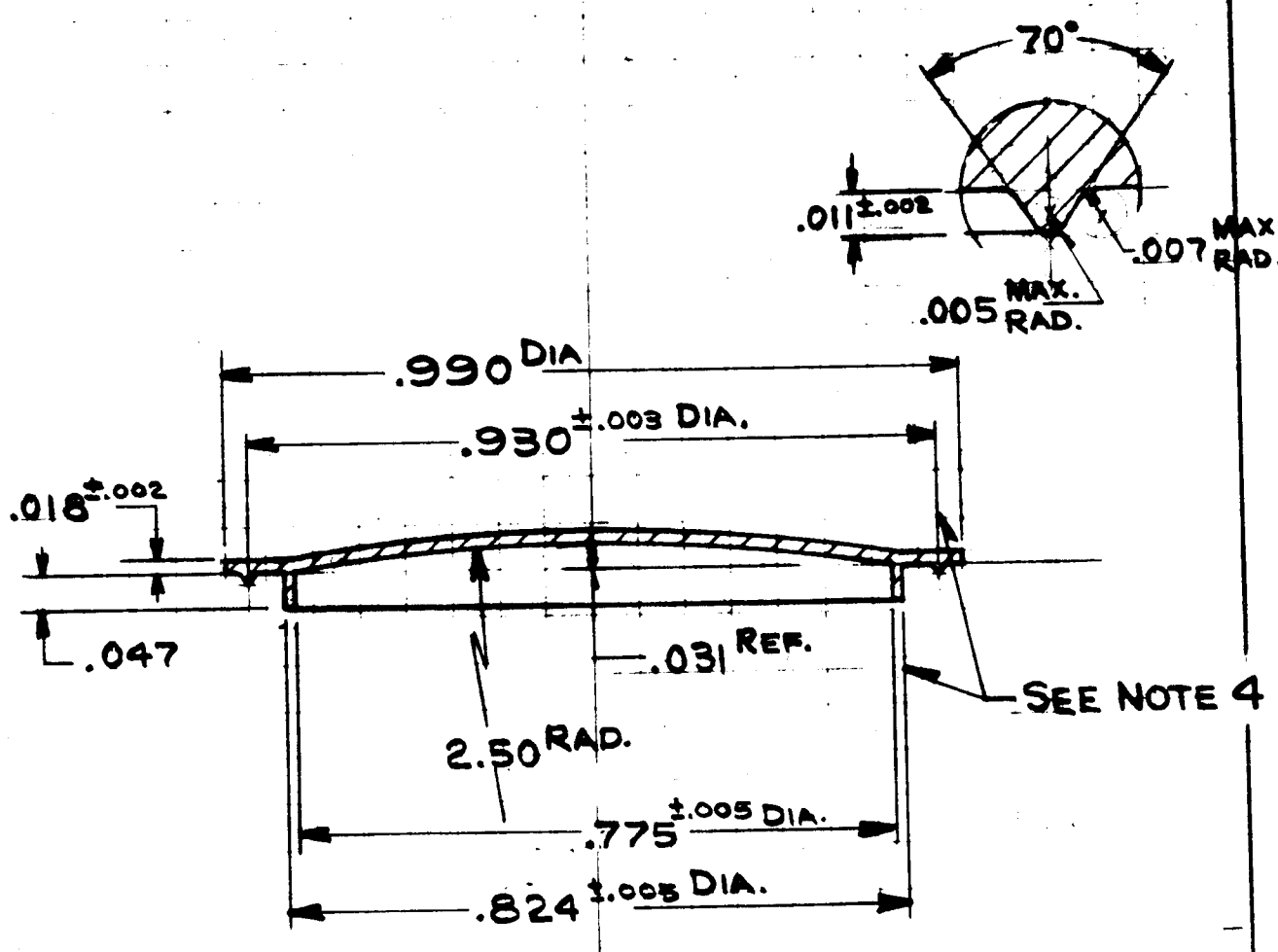


FIGURE 27

Vertical Base Design
(with components)

MATERIAL- STL 10102RX



NOTES:

1. CREST OF WELD PROJECTION MUST BE FLAT WITHIN .002.
2. CREST OF WELD PROJECTION & OPPOSITE FLAT SURFACE MUST BE MUTUALLY PARALLEL WITH NO MORE THAN .002 THICKNESS VARIATION ON ANY INDIVIDUAL PIECE.
3. REMOVE ALL BURRS.
4. MAX. ECCENTRICITY OF THESE DIAMETERS TO O.D. .006 T.I.R.

FIGURE 28: Metal Cap

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